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Maruko

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(45) **Date of Patent: Aug. 16, 2016**

(54) **SEMICONDUCTOR PACKAGE, PRINTED CIRCUIT BOARD SUBSTRATE AND SEMICONDUCTOR DEVICE**

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(73) Assignee: **ROHM CO., LTD.**, Kyoto (JP)

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(21) Appl. No.: **14/716,102**

(22) Filed: **May 19, 2015**

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US 2015/0340335 A1 Nov. 26, 2015

(30) **Foreign Application Priority Data**

May 20, 2014 (JP) 2014-103951

(51) **Int. Cl.**

H01L 23/52	(2006.01)
H01L 23/00	(2006.01)
H01L 23/31	(2006.01)
H01L 23/528	(2006.01)
H05K 1/18	(2006.01)
H05K 1/11	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 24/17*** (2013.01); ***H01L 23/3114*** (2013.01); ***H01L 23/528*** (2013.01); ***H05K 1/111*** (2013.01); ***H05K 1/181*** (2013.01); *H01L 2224/1623* (2013.01); *H01L 2224/16113* (2013.01); *H01L 2224/16227* (2013.01); *H01L 2224/1713* (2013.01); *H01L 2224/17134* (2013.01); *H01L 2224/17179* (2013.01); *H01L 2924/14* (2013.01); *H05K 2201/09418* (2013.01)

(58) **Field of Classification Search**

CPC H01L 24/17; H01L 23/3114; H01L 23/528
USPC 257/786
See application file for complete search history.

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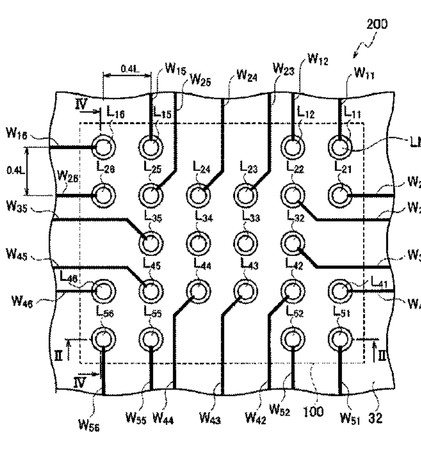
Primary Examiner — Luan C Thai
(74) *Attorney, Agent, or Firm* — Cantor Colburn LLP

(57) **ABSTRACT**

A semiconductor package includes: a semiconductor integrated circuit; an interlayer film disposed on the semiconductor integrated circuit; a rewiring layer disposed on the interlayer film; post electrodes disposed on the rewiring layer; a protective layer which is disposed on the interlayer film and covers the rewiring layer and the post electrodes; and a plurality of balls which is respectively disposed on the post electrodes and is connected to the rewiring layer, wherein balls existing on a wiring path of internal wirings connected to inner lands of a plurality of lands, which is arranged on a printed circuit board substrate to face the plurality of balls and is connectable to the plurality of balls, are non-connected to the rewiring layer.

24 Claims, 29 Drawing Sheets



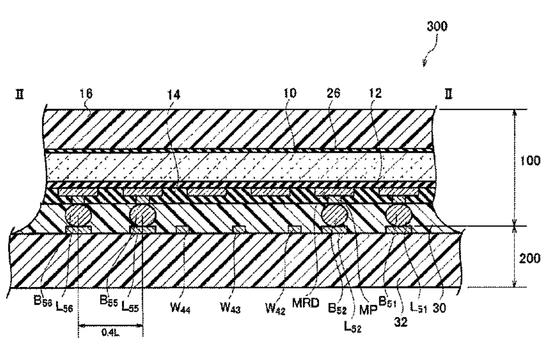
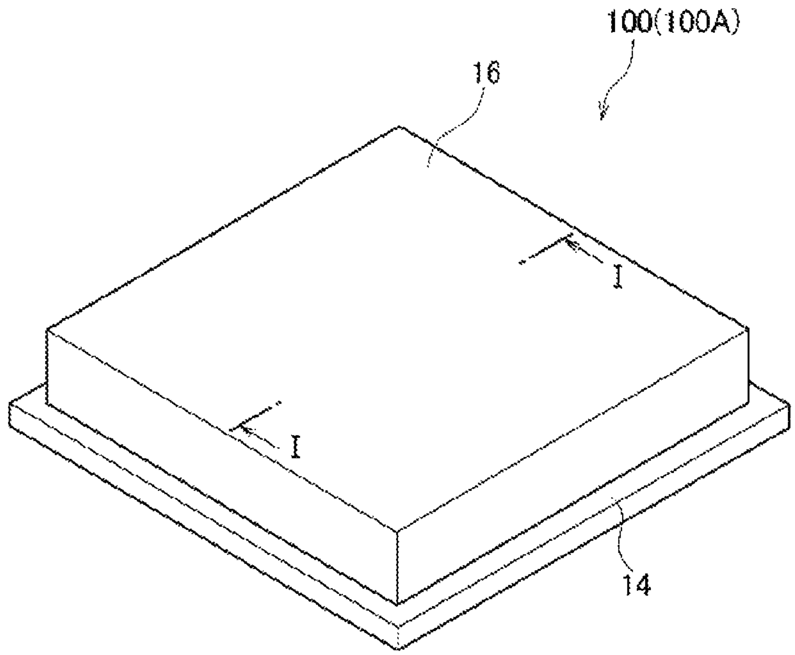


FIG. 1



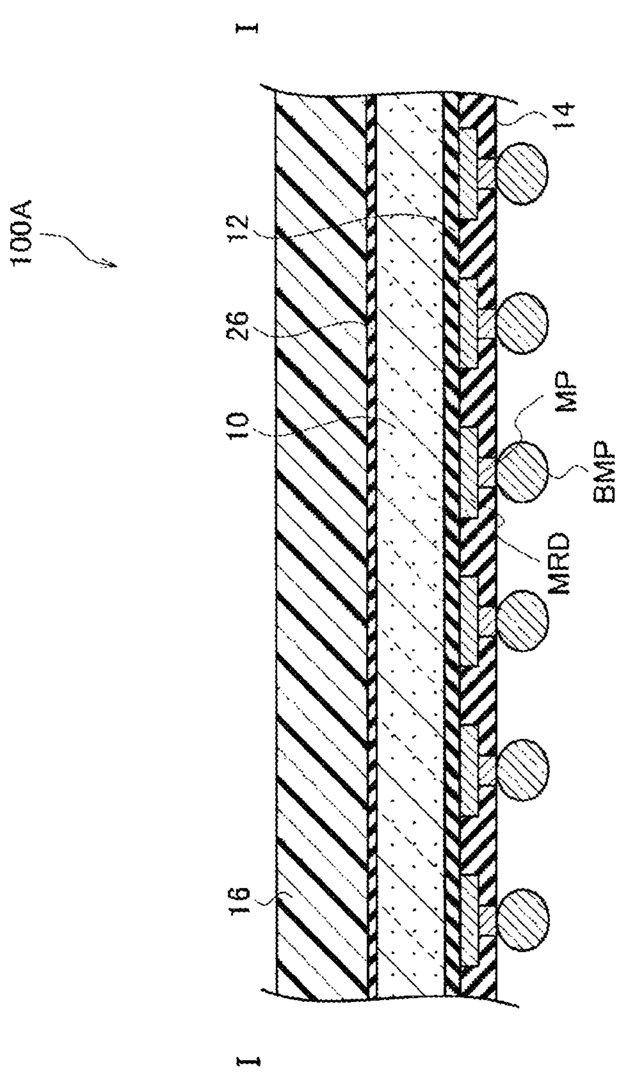


FIG. 2

FIG. 3

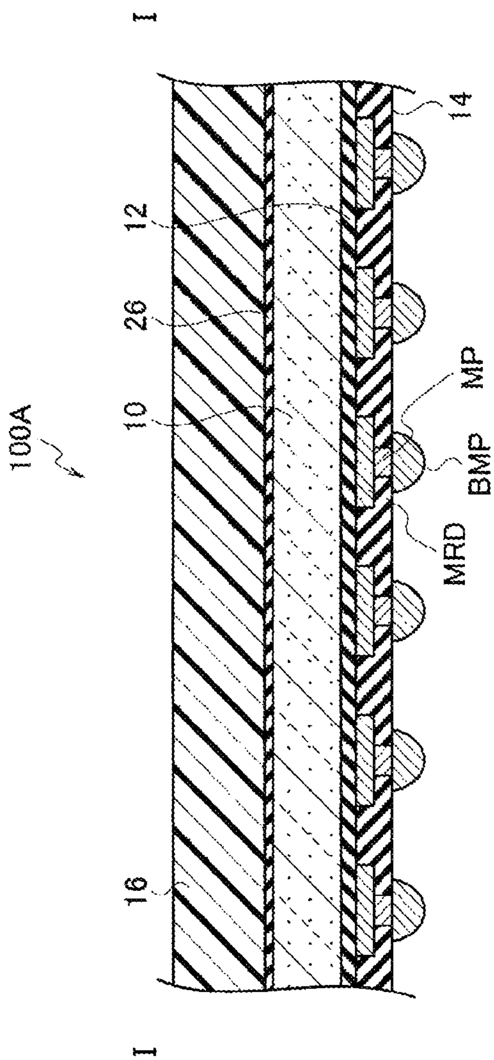


FIG. 4

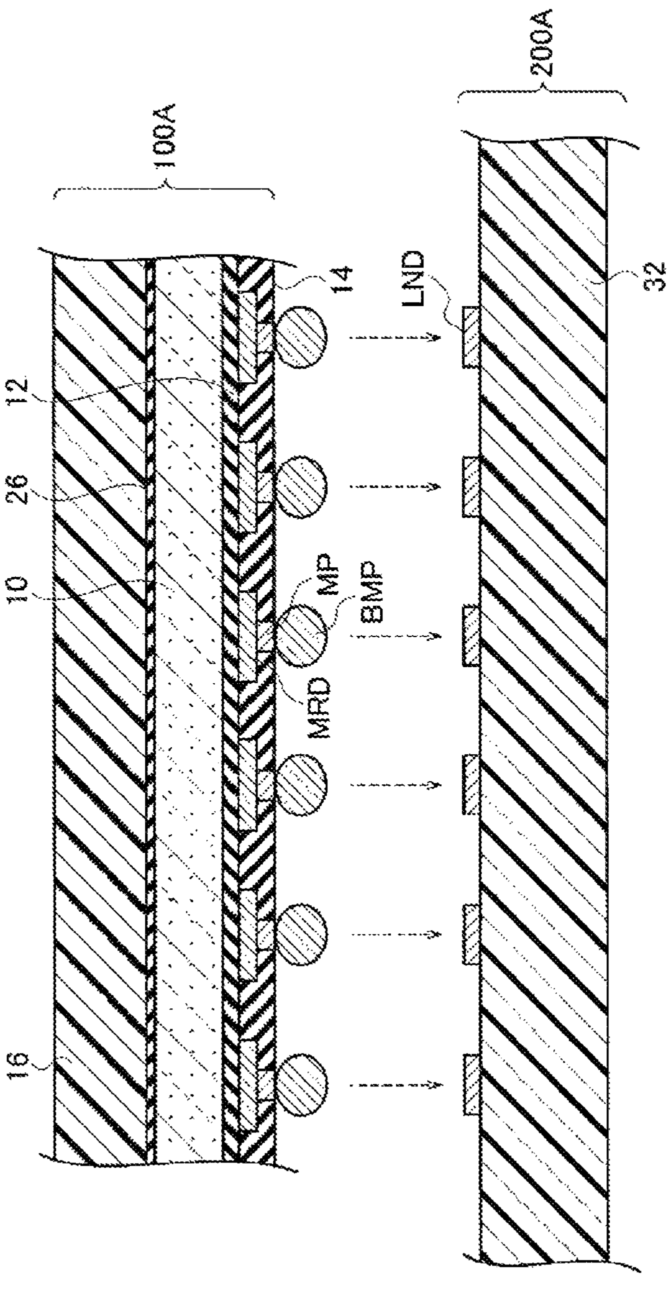


FIG. 5

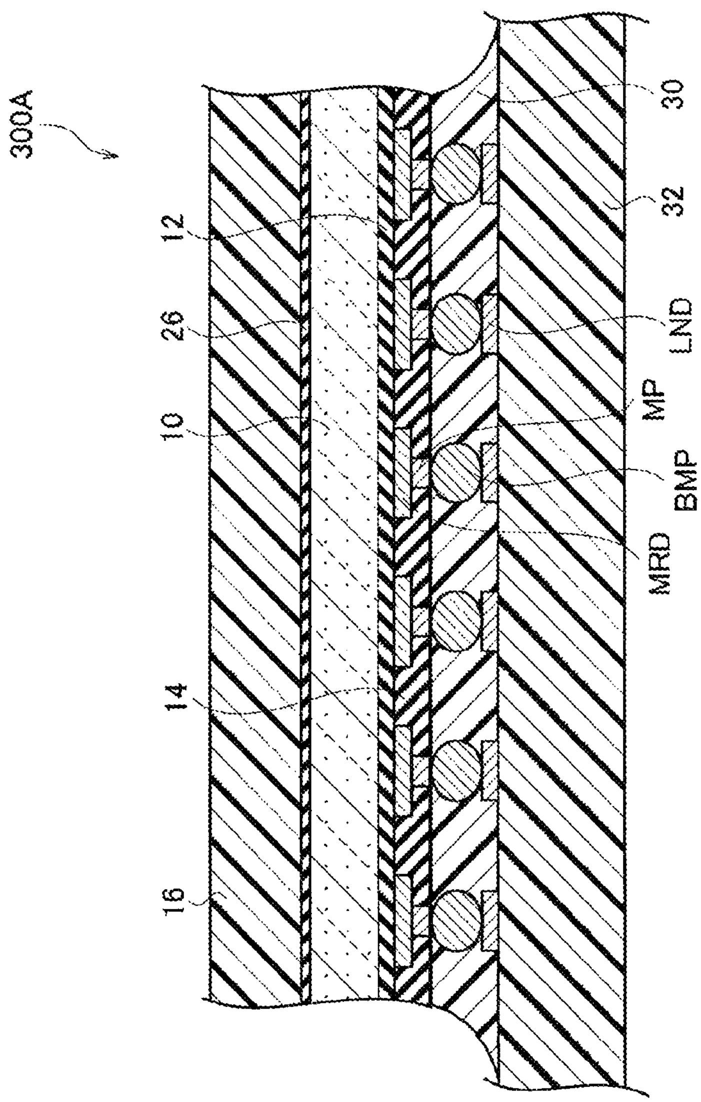


FIG. 6

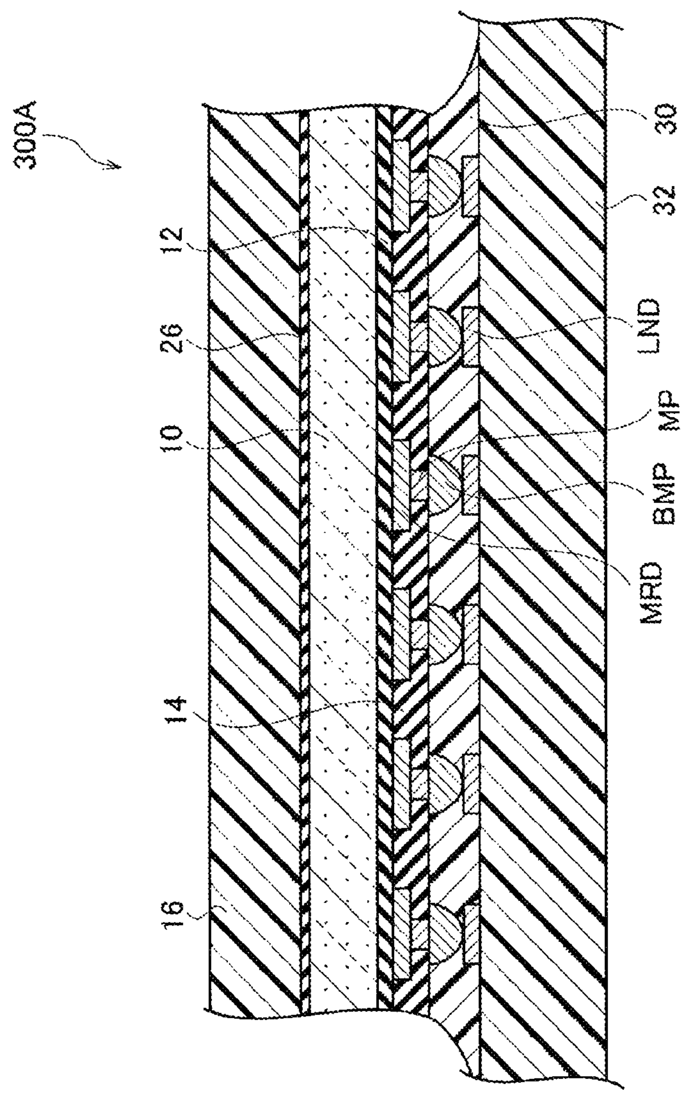


FIG. 7

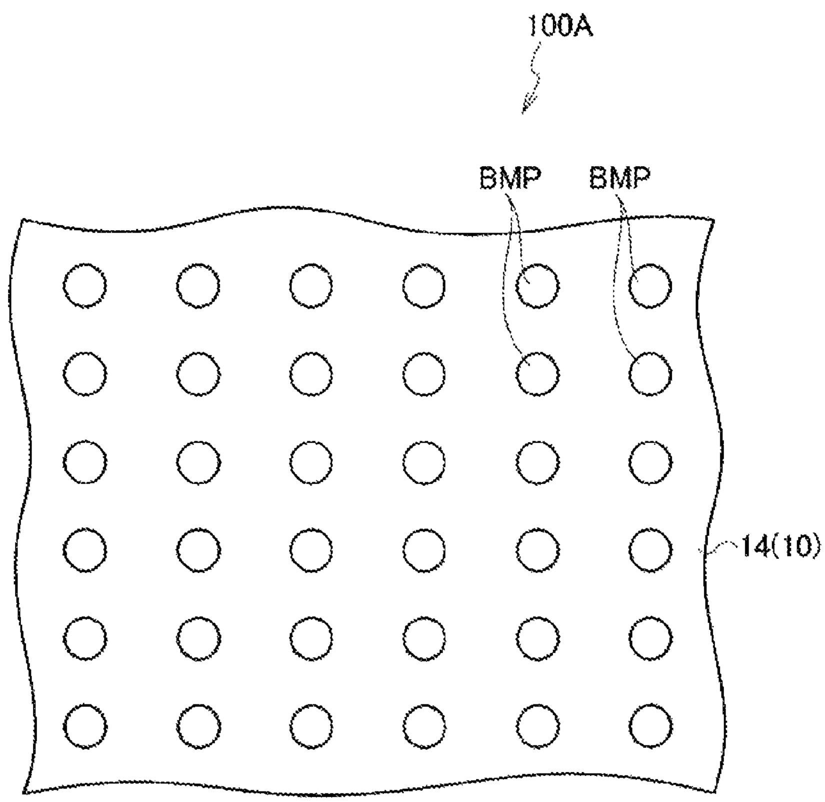


FIG. 8

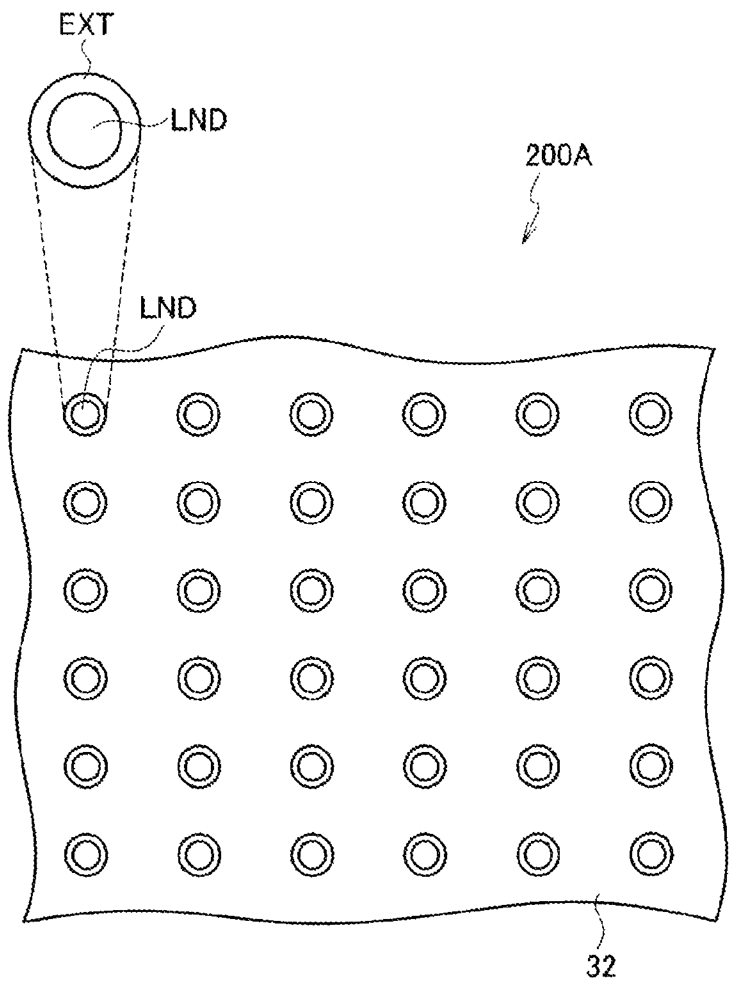


FIG. 9

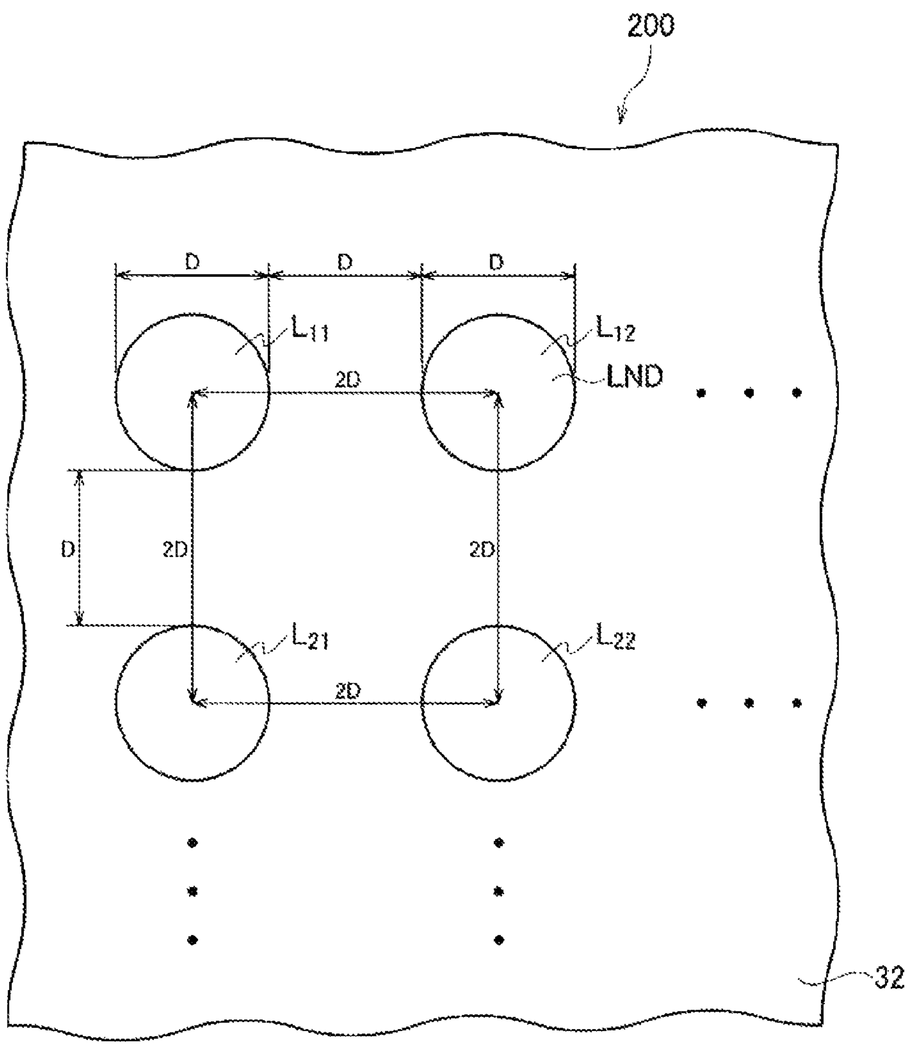


FIG. 10

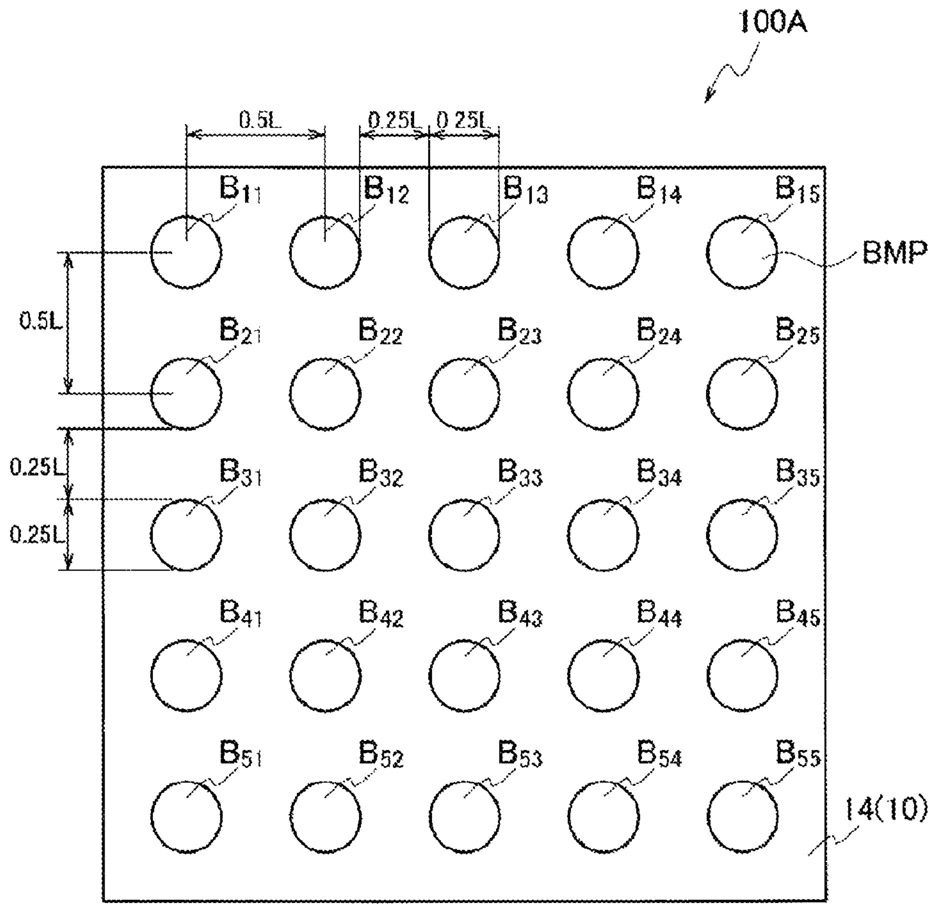

100A
0.5L
0.25L
0.25L
B11
B12
B13
B14
B15
BMP
0.5L
B21
B22
B23
B24
B25
0.25L
0.25L
B31
B32
B33
B34
B35
B41
B42
B43
B44
B45
B51
B52
B53
B54
B55
14(10)

FIG. 11

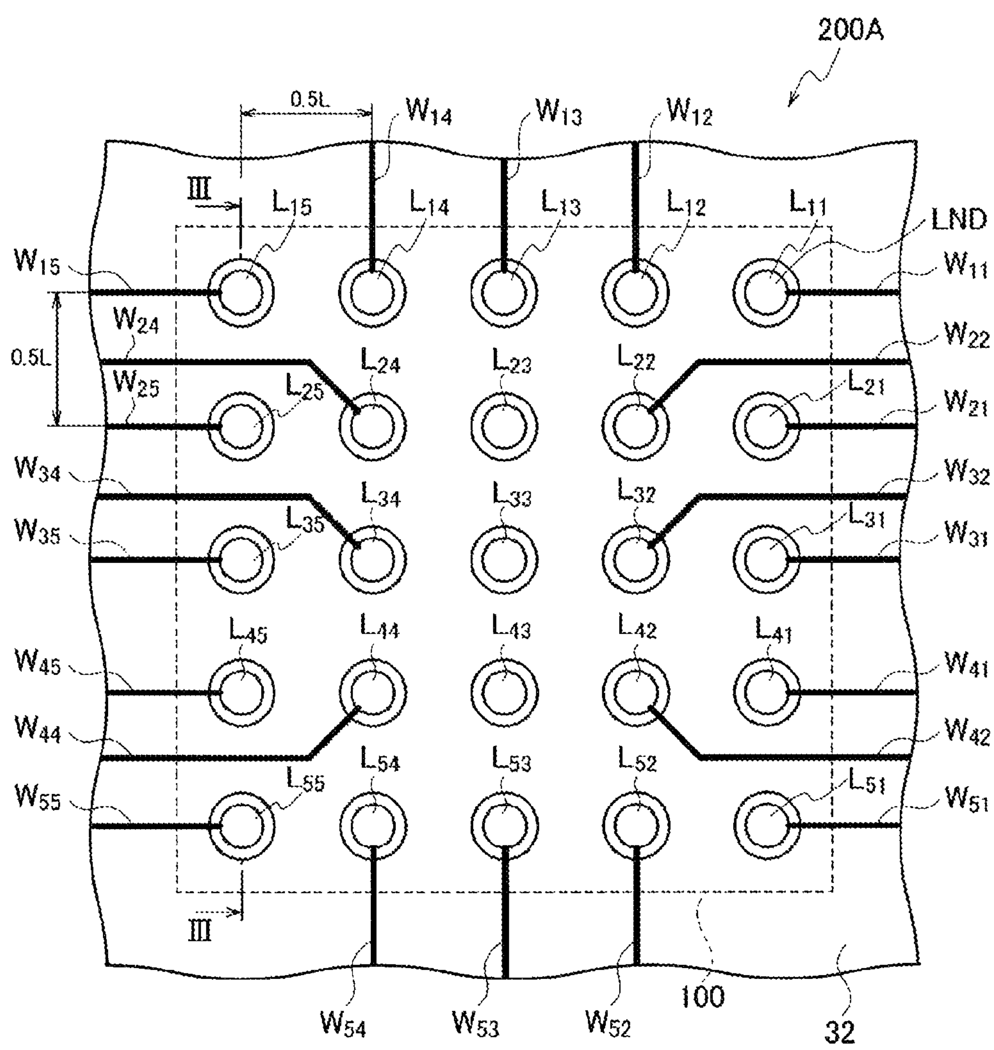

200A
0.5L
W14
W13
W12
III
L15
L14
L13
L12
L11
LND
W15
W11
W24
0.5L
L24
L23
L22
W22
W25
L25
L21
W21
W34
L34
L33
L32
W32
W35
L35
L31
W31
L45
L44
L43
L42
L41
W45
W41
W44
W42
L55
L54
L53
L52
L51
W55
W51
III
W54
W53
W52
100
32

FIG. 12

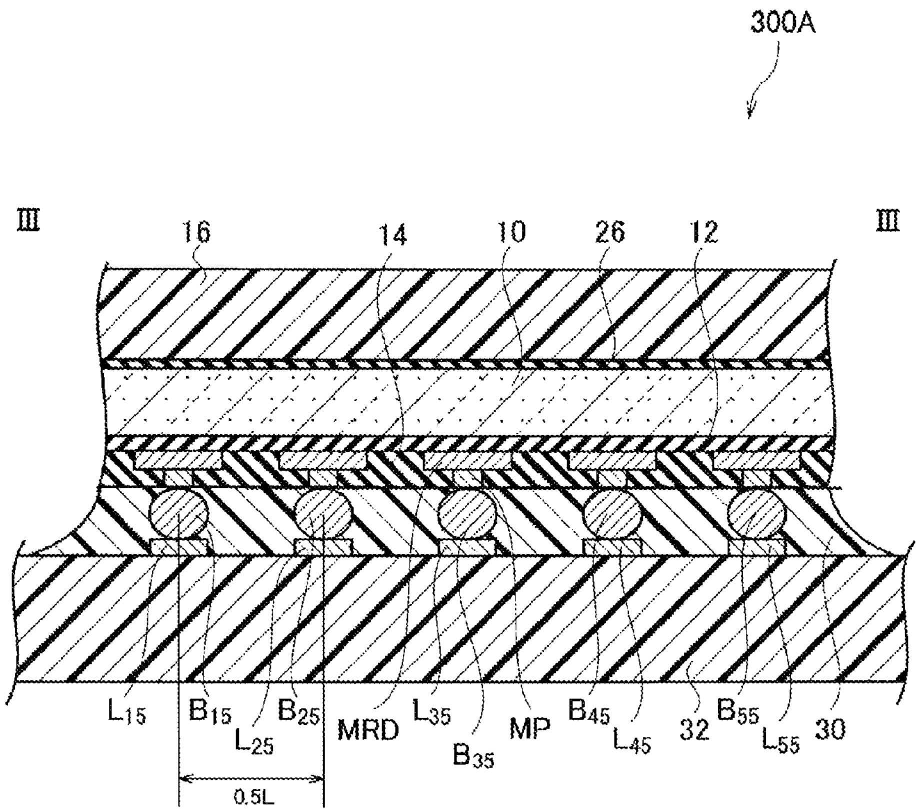

300A
III
III
16
14
10
26
12
L15
B15
L25
B25
MRD
L35
B35
MP
B45
L45
32
B55
L55
30
0.5L

FIG. 13

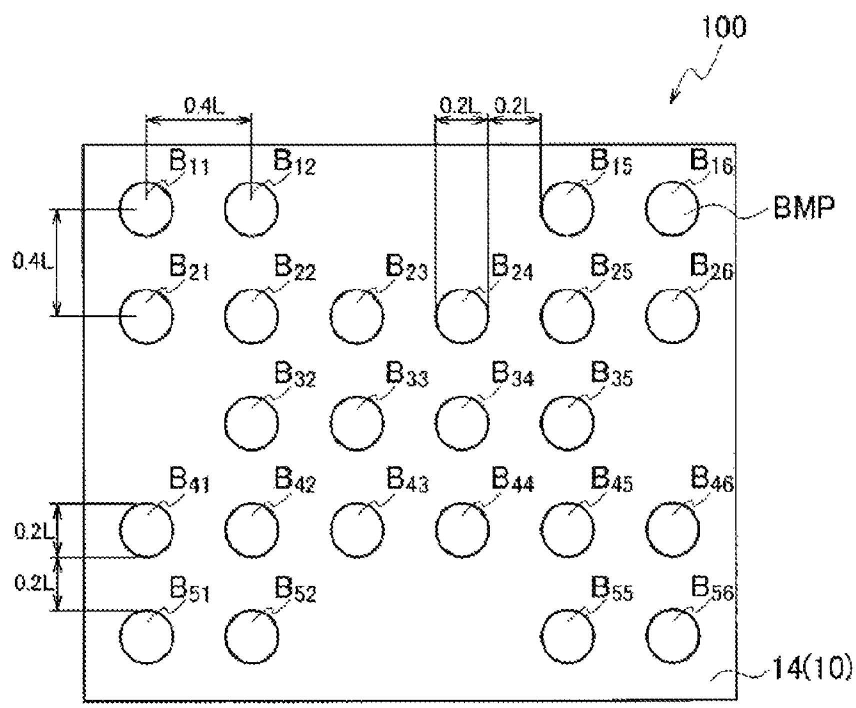
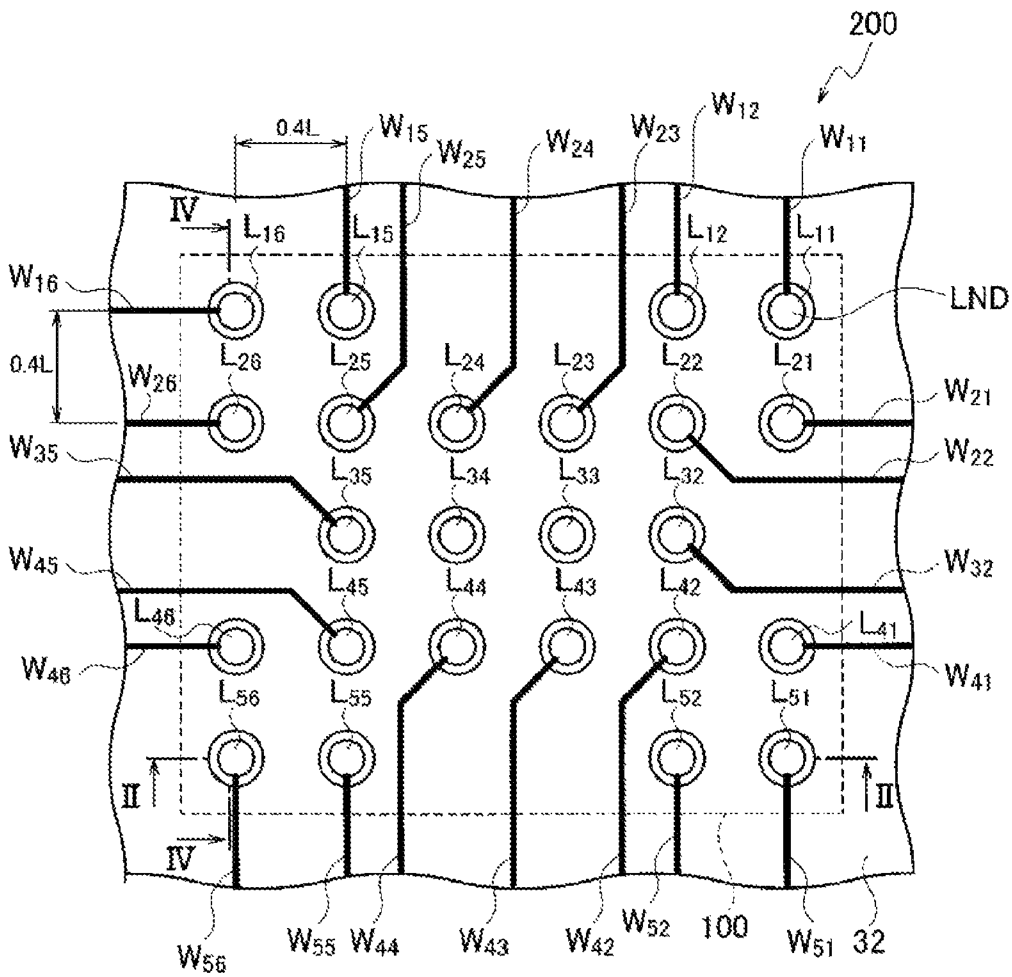
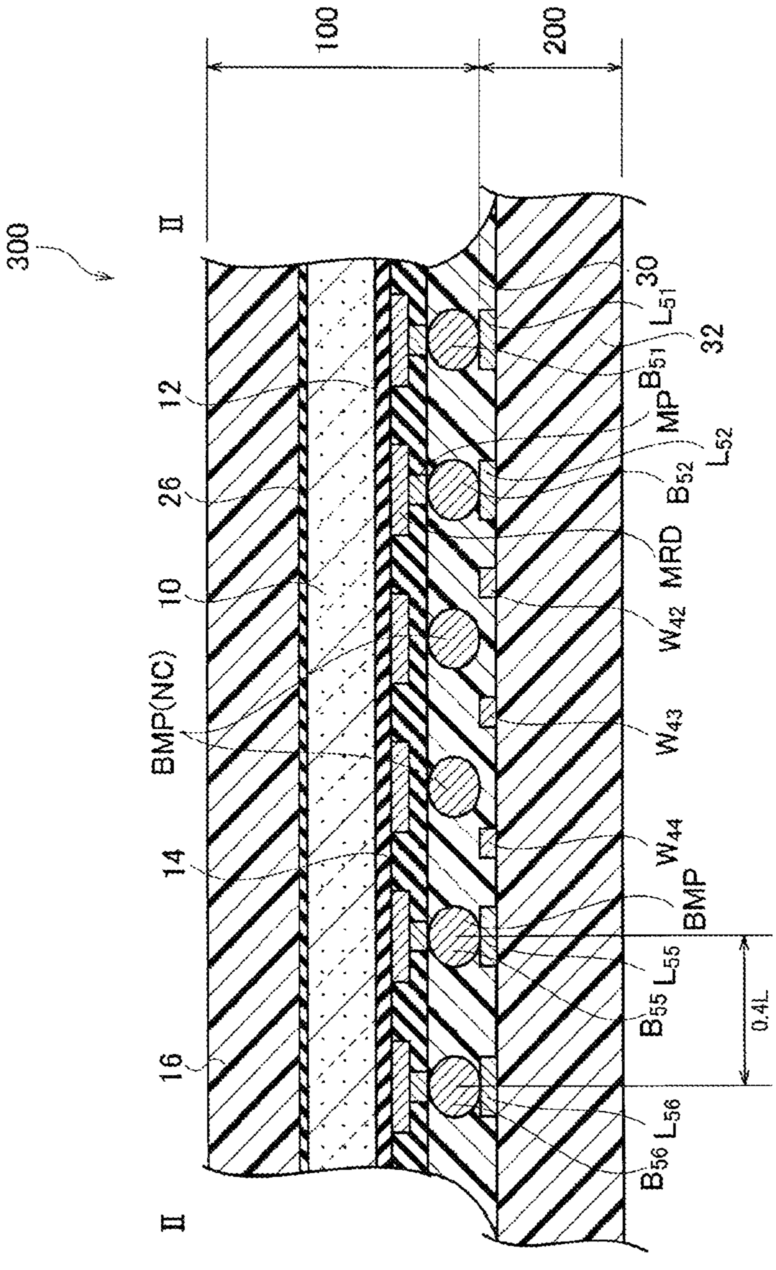

100
0.4L
0.2L
0.2L
B11
B12
B15
B16
BMP
0.4L
B21
B22
B23
B24
B25
B26
B32
B33
B34
B35
B41
B42
B43
B44
B45
B46
0.2L
0.2L
B51
B52
B55
B56
14(10)

FIG. 14



200
0.4L
W15
W25
W24
W23
W12
W11
IV
L16
L15
L12
L11
W16
LND
0.4L
L26
L25
L24
L23
L22
L21
W26
W21
W35
W22
L35
L34
L33
L32
W45
W32
L45
L44
L43
L42
L46
L41
W46
W41
L56
L55
L52
L51
II
II
IV
W56
W55
W44
W43
W42
W52
100
W51
32

FIG. 15



100
200
300
II
II
12
26
10
BMP(NC)
14
16
30
L_{51}
32
B_{51}
MP
B_{52}
L_{52}
MRD
W_{42}
W_{43}
W_{44}
BMP
L_{55}
B_{55}
0.4L
L_{56}
B_{56}

FIG. 16

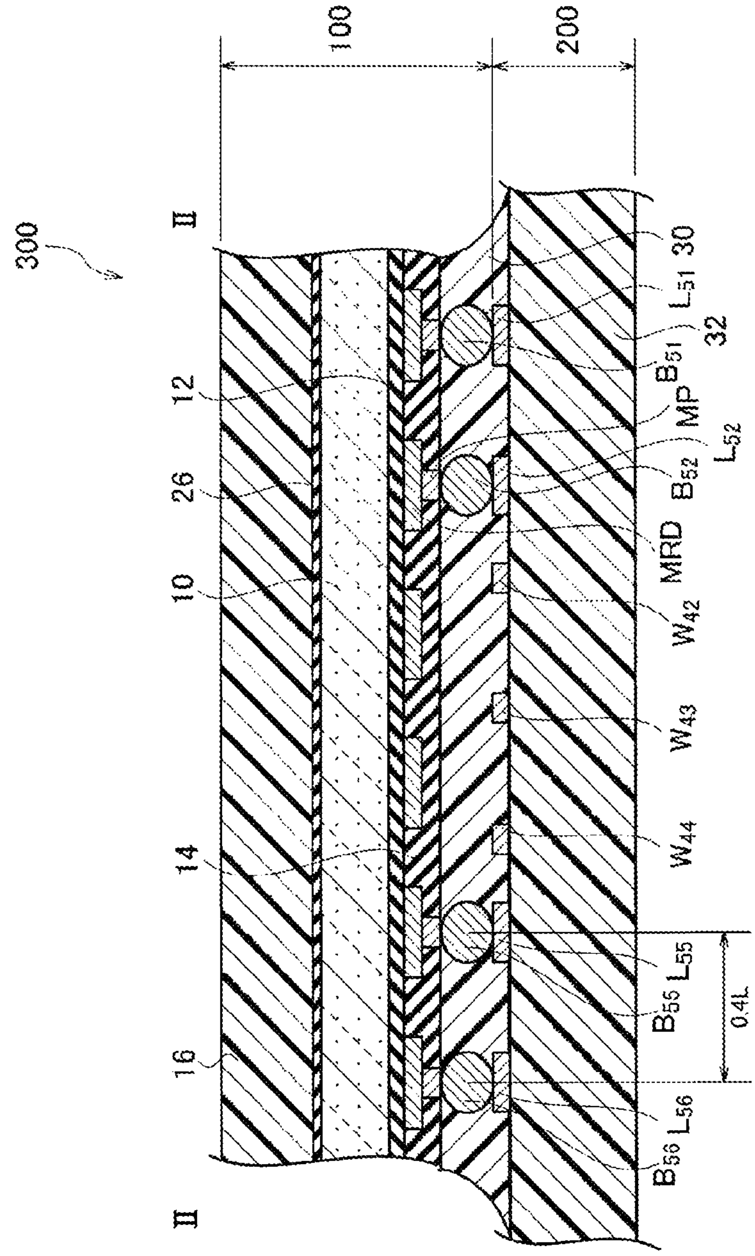

300
100
200
II
II
12
26
10
14
16
30
32
L_{51}
B_{51}
MP
L_{52}
B_{52}
MRD
W_{42}
W_{43}
W_{44}
B_{55}
L_{55}
0.4L
B_{56}
L_{56}

FIG. 17A

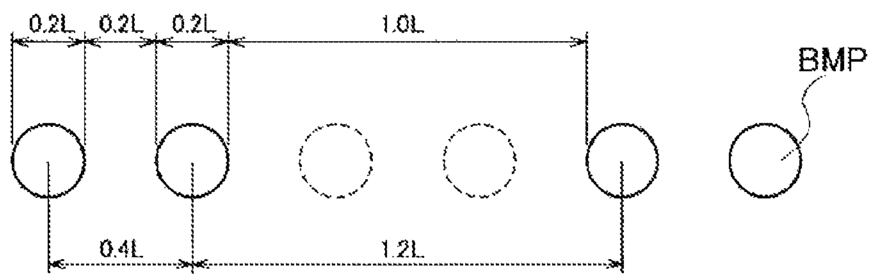


FIG. 17B

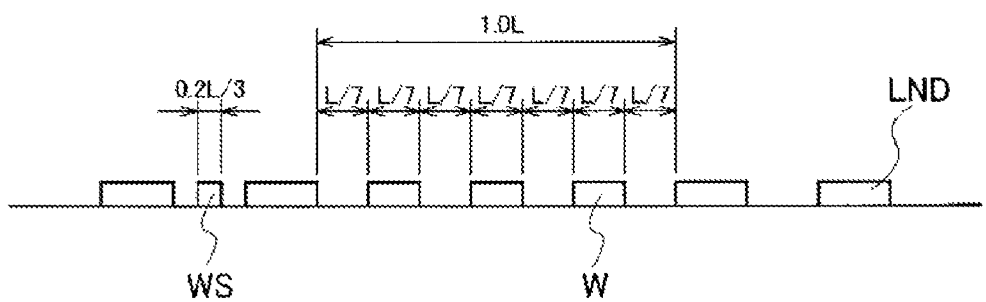


FIG. 18

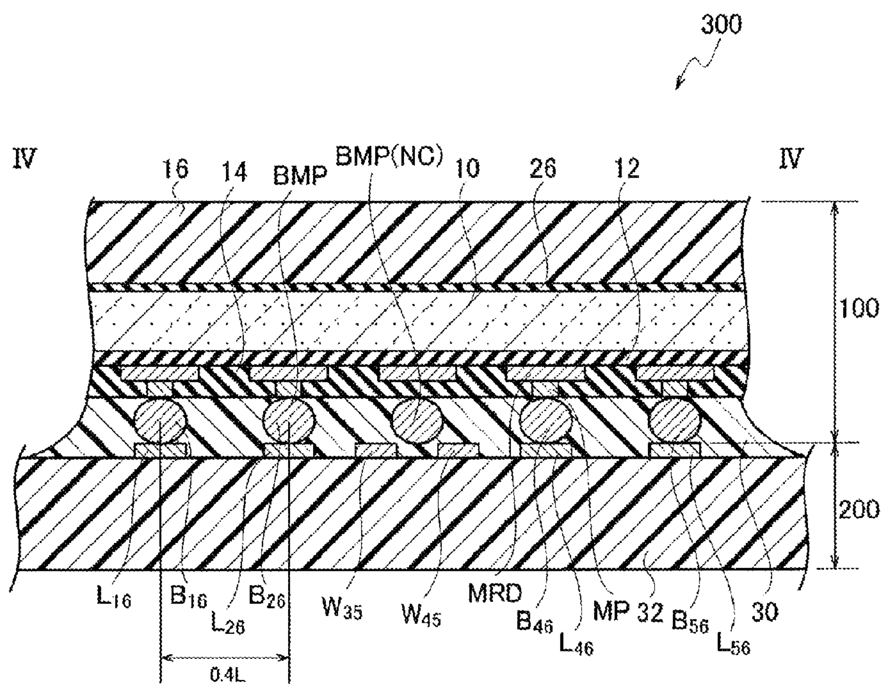

300
IV
16
14
BMP
BMP(NC)
10
26
12
IV
100
200
L16
B16
L26
B26
W35
W45
MRD
B46
L46
MP
32
B56
L56
30
0.4L

FIG. 19

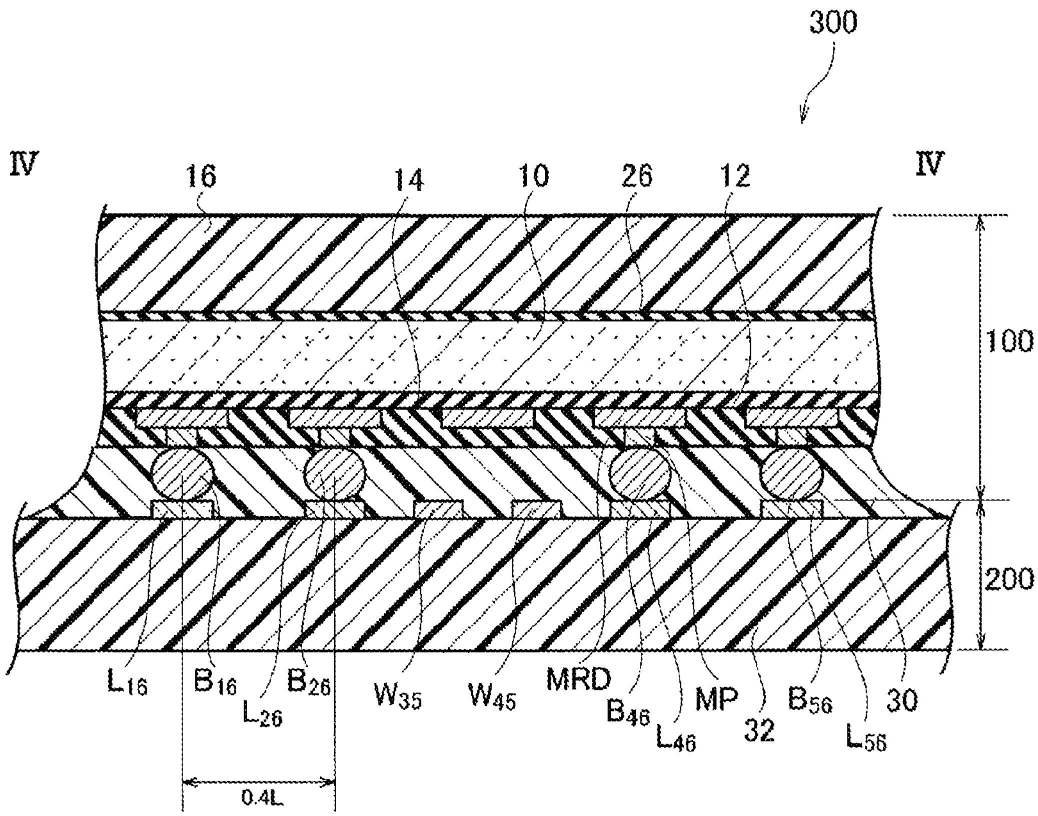


FIG. 20A

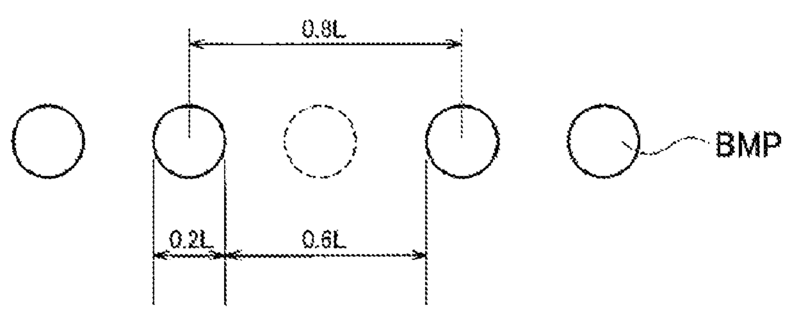


FIG. 20B

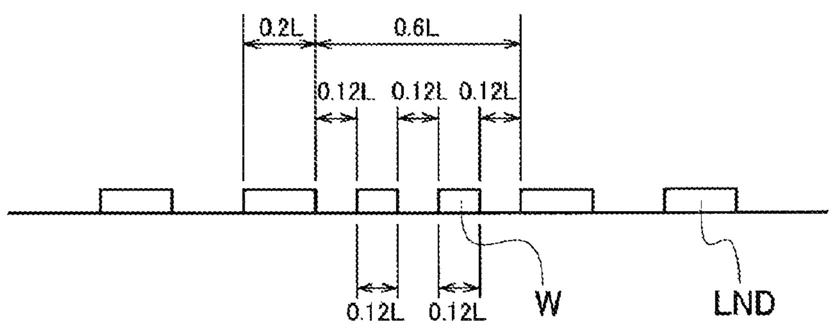


FIG. 21

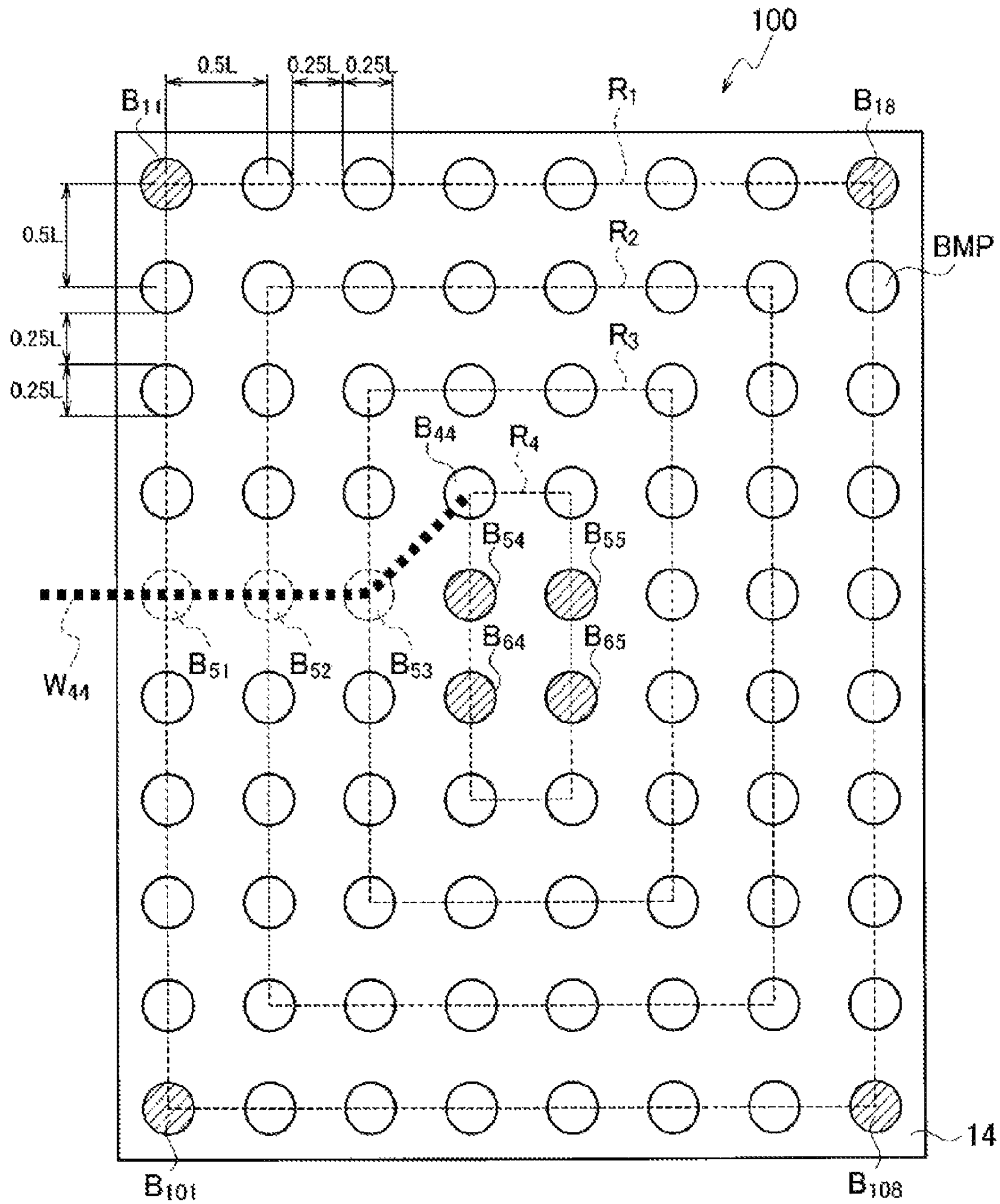

100
0.5L
0.25L
0.25L
B11
R1
B18
0.5L
R2
BMP
0.25L
R3
0.25L
B44
R4
B54
B55
B64
B65
W44
B51
B52
B53
14
B101
B108

FIG. 22

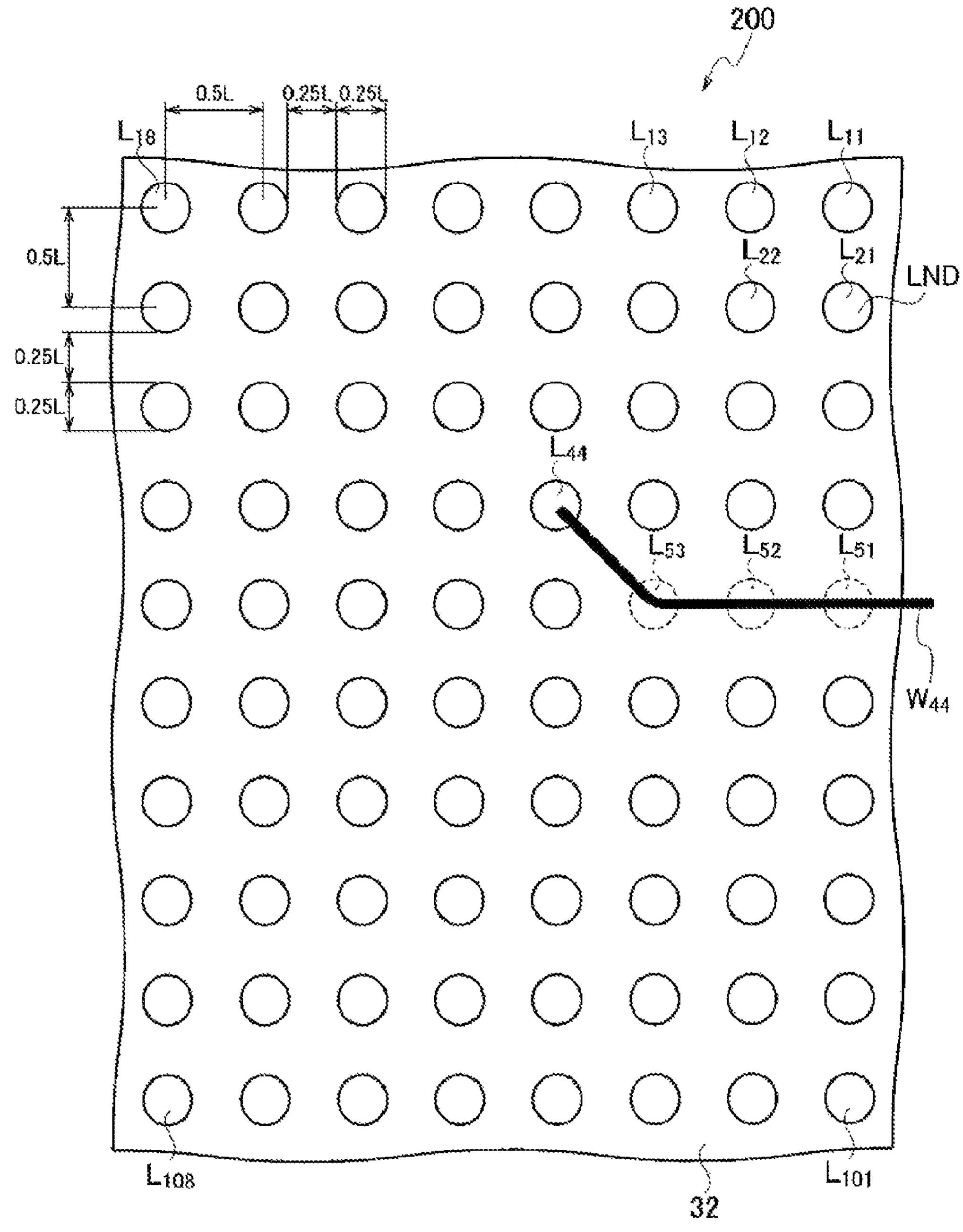
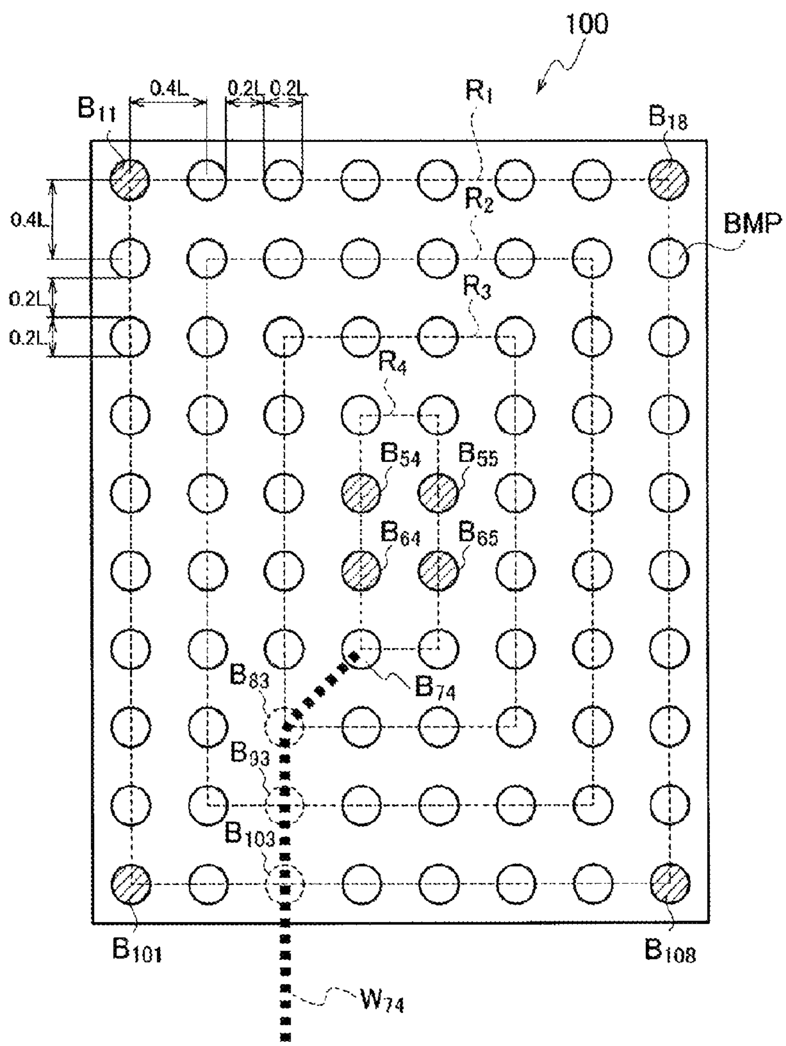

200
0.5L
0.25L
0.25L
L_{18}
L_{13}
L_{12}
L_{11}
0.5L
L_{22}
L_{21}
LND
0.25L
0.25L
L_{44}
L_{53}
L_{52}
L_{51}
W_{44}
L_{108}
L_{101}
32

FIG. 23



100
0.4L
0.2L
0.2L
R_1
B_{11}
B_{18}
0.4L
R_2
BMP
0.2L
0.2L
R_3
R_4
B_{54}
B_{55}
B_{64}
B_{65}
B_{83}
B_{74}
B_{93}
B_{103}
B_{101}
B_{108}
W_{74}

FIG. 24

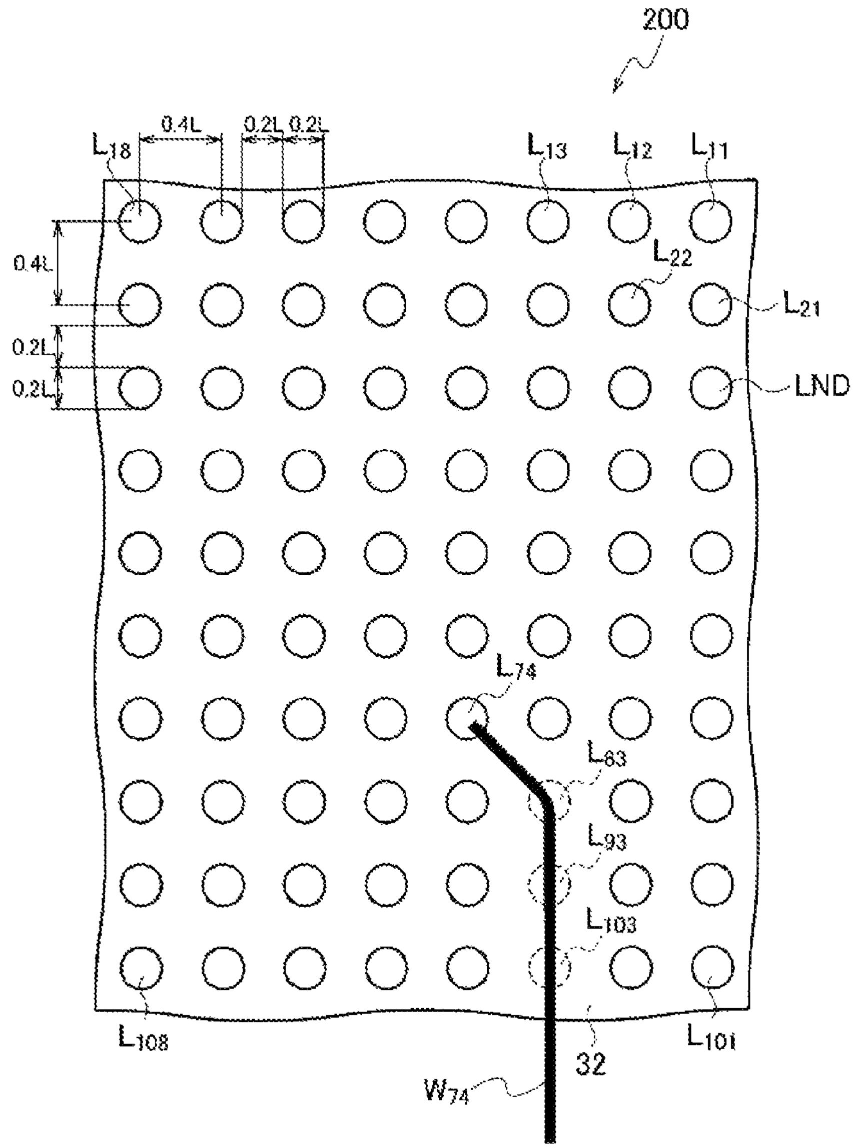
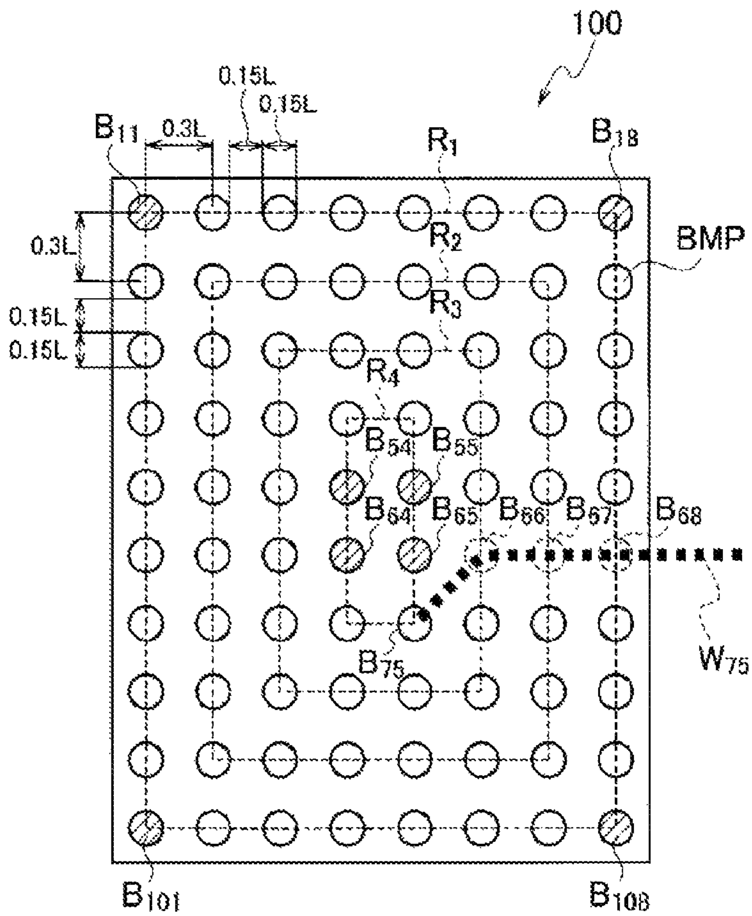
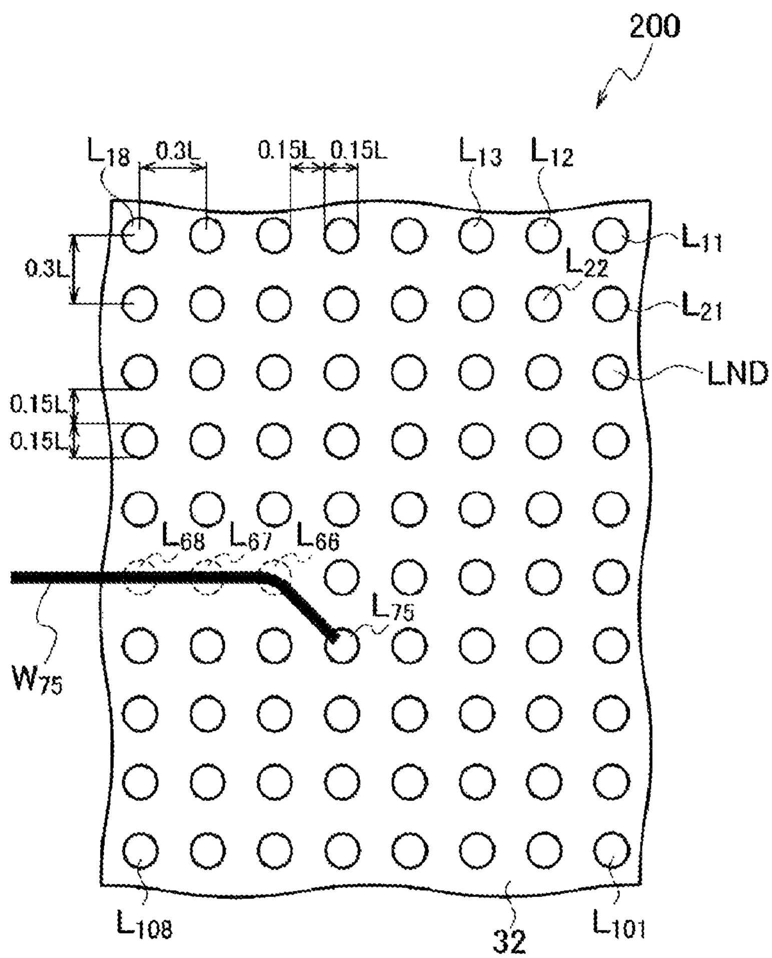

200
0.4L
0.2L
0.2L
L18
L13
L12
L11
L22
L21
LND
L74
L63
L93
L103
L108
L101
32
W74

FIG. 25



100
0.15L
0.15L
B_{11}
0.3L
R_1
B_{18}
0.3L
R_2
BMP
0.15L
R_3
0.15L
R_4
B_{54}
B_{55}
B_{64}
B_{65}
B_{66}
B_{67}
B_{68}
B_{75}
W_{75}
B_{101}
B_{108}

FIG. 26



200
L18
0.3L
0.15L
0.15L
L13
L12
L11
L22
L21
LND
0.3L
0.15L
0.15L
L68
L67
L66
L75
W75
L108
32
L101

FIG. 27A

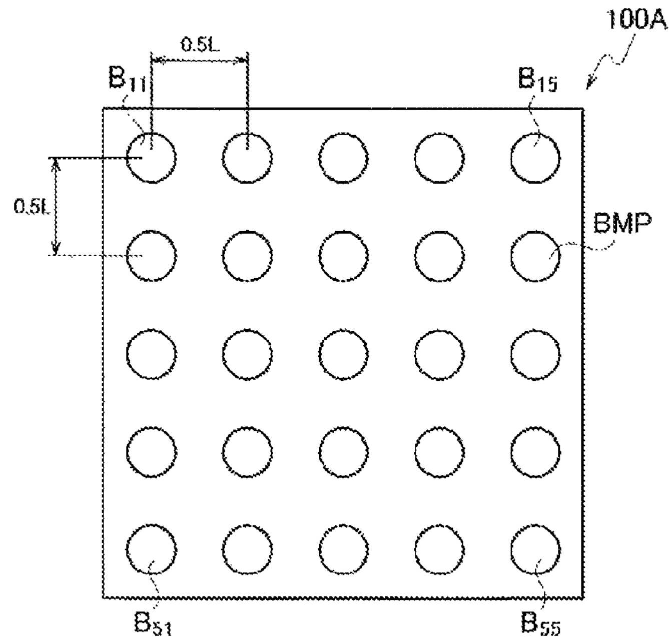


FIG. 27B

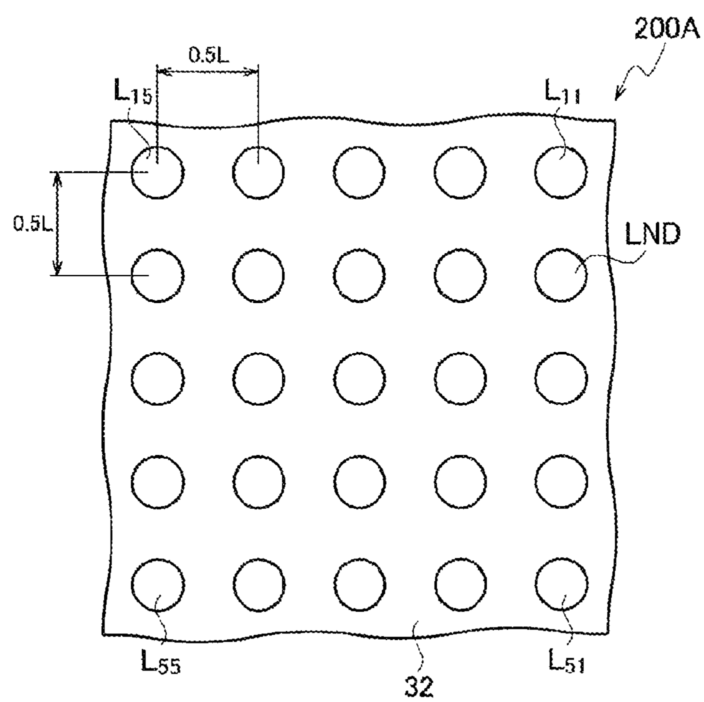


FIG. 28

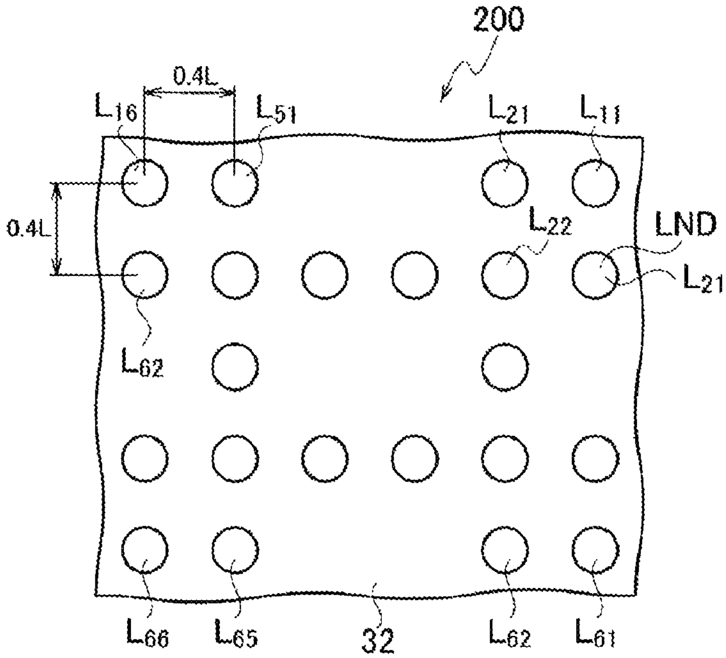

200
0.4L
L16
L51
L21
L11
0.4L
L22
LND
L21
L62
L66
L65
32
L62
L61

FIG. 29

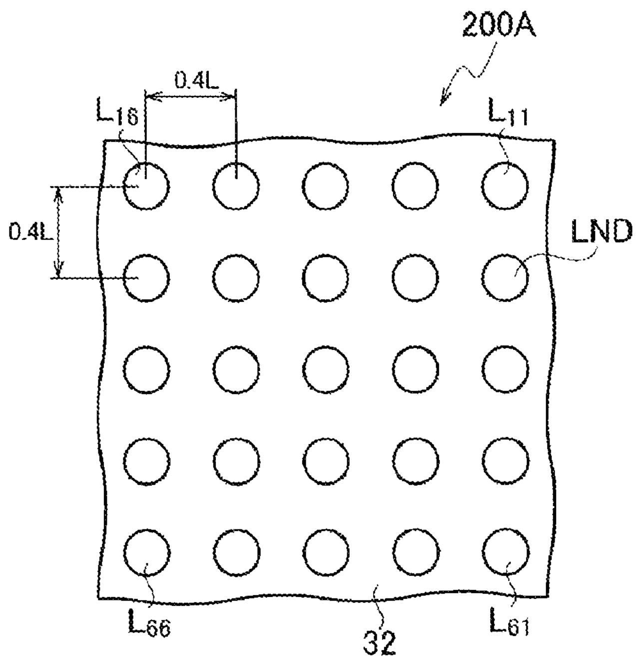
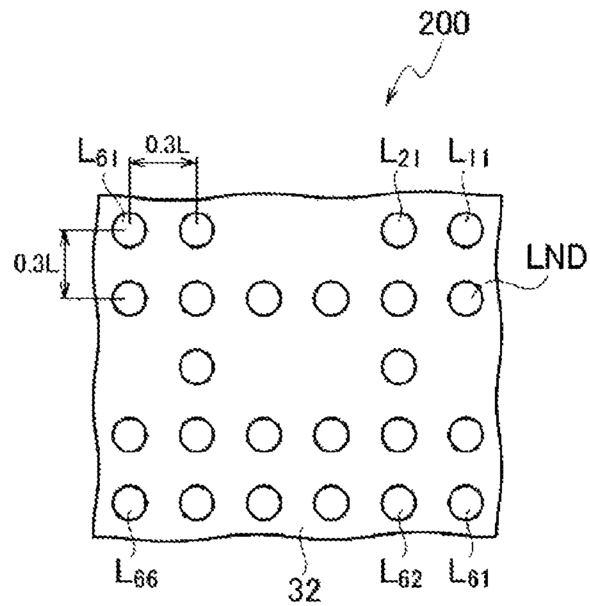

200A
0.4L
L16
L11
0.4L
LND
L66
32
L61

FIG. 30



SEMICONDUCTOR PACKAGE, PRINTED CIRCUIT BOARD SUBSTRATE AND SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

The present invention claims priority under 35 U.S.C. §119 to Japanese Application No. 2014-103951, filed on May 20, 2014, the entire content of which is incorporated herein by reference.

TECHNICAL FIELD

The present disclosure relates to a semiconductor package, a printed circuit board substrate and a semiconductor device, and more particularly relates to a semiconductor package with a structure where balls are removed or made non-connective for substrate wiring in a grid array package such as BGA (Ball Grid Array)/LGA (Land Grid Array) or the like, a printed circuit board substrate on which the semiconductor package is mounted, and a semiconductor device including the printed circuit board substrate and the semiconductor package mounted on the printed circuit board substrate.

BACKGROUND

As a package structure facilitating miniaturization, high functionality and high performance of semiconductor integrated circuit chips, there has been proposed a grid array package such as WL-CSP (Wafer Level Chip Scale Package) or BGA/LGA.

Typically, when a package such as WL-CSP/BGA/LGA or the like is mounted on a printed circuit board (hereinafter, referred to as a "PCB substrate"), in order to pass wirings between lands corresponding to balls on the PCB substrate, wiring pitches get narrow and the cost of the PCB substrate increases.

In particular, in the case of WL-CSP, the relationship between a chip size and a ball size has an opposite relationship. That is, when the chip size is reduced, the ball pitch is narrowed, which results in increase in the PCB substrate cost. Conversely, when the ball pitch is widened, the chip size is increased, which results in increase in the chip cost.

SUMMARY

The present disclosure provides some embodiments of a semiconductor package which is capable of reducing the chip size and eliminating a need to miniaturize the wiring width on a printed circuit board substrate and can be easily mounted, a printed circuit board substrate on which the semiconductor package is mounted, and a semiconductor device including the printed circuit board substrate and the semiconductor package mounted on the printed circuit board substrate.

According to one embodiment of the present disclosure, there is provided a semiconductor package including: a semiconductor integrated circuit; an interlayer film disposed on the semiconductor integrated circuit; a rewiring layer disposed on the interlayer film; post electrodes disposed on the rewiring layer; a protective layer which is disposed on the interlayer film and covers the rewiring layer and the post electrodes; and a plurality of balls which is respectively disposed on the post electrodes and is connected to the rewiring layer, wherein balls existing on a wiring path of internal wirings connected to inner lands of a plurality of lands, which is arranged on a printed circuit board substrate to face the plurality of balls and is connectable to the plurality of balls, are non-connected to the rewiring layer.

According to another embodiment of the present disclosure, there is provided a semiconductor package including: a semiconductor integrated circuit; an interlayer film disposed on the semiconductor integrated circuit; a rewiring layer disposed on the interlayer film; post electrodes disposed on the rewiring layer; a protective layer which is disposed on the interlayer film and covers the rewiring layer and the post electrodes; and a plurality of balls which is respectively disposed on the post electrodes and is connected to the rewiring layer, wherein balls existing on a wiring path of internal wirings connected to inner lands of a plurality of lands, which is arranged on a printed circuit board substrate to face the plurality of balls and is connectable to the plurality of balls, are removed.

According to still another embodiment of the present disclosure, there is provided a printed circuit board substrate including: an insulating substrate; a plurality of lands which is arranged on the insulating substrate to face a plurality of balls of a semiconductor package and is respectively connectable to the plurality of balls; and wirings which are arranged on the insulating substrate and are respectively connected to the plurality of lands, wherein lands existing on a wiring path of internal wirings, which are connected to lands arranged in an inside on the insulating substrate, are non-connected to a rewiring layer of the semiconductor package.

According to still another embodiment of the present disclosure, there is provided a printed circuit board substrate including: an insulating substrate; a plurality of lands which is arranged on the insulating substrate to face a plurality of balls of a semiconductor package and is respectively connectable to the plurality of balls; and wirings which are arranged on the insulating substrate and are respectively connected to the plurality of lands, wherein lands existing on a wiring path of internal wirings, which are connected to lands arranged in the inside on the insulating substrate, are removed.

According to still another embodiment of the present disclosure, there is provided a semiconductor device including: a semiconductor package including a semiconductor integrated circuit, an interlayer film disposed on the semiconductor integrated circuit, a rewiring layer disposed on the interlayer film, post electrodes disposed on the rewiring layer, a protective layer which is disposed on the interlayer film and covers the rewiring layer and the post electrodes, and a plurality of balls which is respectively disposed on the post electrodes and is connected to the rewiring layer; and a printed circuit board substrate including an insulating substrate, a plurality of lands which is arranged on the insulating substrate to face the plurality of balls and is respectively connectable to the plurality of balls, and wirings which are arranged on the insulating substrate and are respectively connected to the plurality of lands, wherein balls existing on a wiring path of internal wirings, which are connected to lands arranged in the inside on the insulating layer, are non-connected to the rewiring layer.

According to still another embodiment of the present disclosure, there is provided a semiconductor device including: a semiconductor package including a semiconductor integrated circuit, an interlayer film disposed on the semiconductor integrated circuit, a rewiring layer disposed on the interlayer film, post electrodes disposed on the rewiring layer, a protective layer which is disposed on the interlayer film and covers the rewiring layer and the post electrodes, and a plurality of balls which is respectively disposed on the post electrodes and is connected to the rewiring layer; and a printed circuit board substrate including an insulating substrate, a plurality of lands which is arranged on the insulating substrate to face the plurality of balls and is respectively connectable to the plurality of balls, and wirings which are arranged on the insulating substrate and are respectively connected to the plurality of lands, wherein balls existing on a wiring path of internal wirings, which are connected to lands arranged in the inside on the insulating layer, are removed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic bird's-eye view of a semiconductor package according to the basic technique, which is seen from a front surface side facing a surface on which solder bumps are formed.

FIG. **2** is a schematic sectional view taken along line I-I in FIG. **1**, showing an example of solder bumps formed of BGA.

FIG. **3** is a schematic sectional view taken along line I-I in FIG. **1**, showing an example of solder bumps formed of LGA.

FIG. **4** is a schematic sectional view showing a state of disposing the semiconductor package according to the basic technique on a PCB substrate.

FIG. **5** is a schematic sectional view of a semiconductor device in which the semiconductor package according to the basic technique is disposed on a PCB substrate.

FIG. **6** is a schematic sectional view of another example of the semiconductor device in which the semiconductor package according to the basic technique is disposed on the PCB substrate.

FIG. **7** is a schematic plan view of the semiconductor package according to the basic technique, showing a surface of a side on which solder bumps are formed.

FIG. **8** is a schematic plan view showing a surface of a side in which the lands LND of the PCB substrate mounting the semiconductor package are formed according to the basic technique shown in FIG. **7**.

FIG. **9** is a schematic enlarged view for explaining arrangements of lands LND on the PCB substrate.

FIG. **10** is a planar pattern configuration view of the semiconductor package according to the basic technique, showing BGA with balls arranged at a 0.5L pitch on a surface of a side on which solder bumps are formed.

FIG. **11** is a planar pattern configuration view of lands LND arranged at a 0.5L pitch on a land LND forming surface of the PCB substrate on which the semiconductor package shown in FIG. **10** according to the basic technique is mounted, and wirings W connected to the lands LND.

FIG. **12** is a schematic sectional view of a semiconductor device in which a semiconductor package according to the basic technique is disposed on a PCB substrate, showing a cut section corresponding to line III-III in FIG. **11**.

FIG. **13** is a planar pattern configuration view of a semiconductor package according to an embodiment, showing BGA with balls arranged at a 0.4L pitch on a surface of a side on which solder bumps are formed.

FIG. **14** is a planar pattern configuration view of lands LND arranged at a 0.4L pitch on a land LND forming surface of the PCB substrate on which the semiconductor package shown in FIG. **13** according to an embodiment is mounted, and wirings W connected respectively to the lands LND.

FIG. **15** is a schematic sectional view of a semiconductor device in which a semiconductor package according to an embodiment is mounted on a PCB substrate, showing a cut section corresponding to line II-II in FIG. **14** (an example where balls BMP (NC) are non-connected to a rewiring layer MRD).

FIG. **16** is a schematic sectional view of a semiconductor device in which a semiconductor package according to a first embodiment is disposed on a PCB substrate, showing a cut section corresponding to line II-II in FIG. **14** (an example where BMPs are removed).

FIG. **17**A is a schematic view for explaining a pitch length of the balls corresponding to FIG. **15** or **16** and FIG. **17**B is a schematic view for explaining a pitch length of lands LND and wirings corresponding to FIG. **17**A.

FIG. **18** is a schematic sectional view of a semiconductor device in which a semiconductor package according to an embodiment is mounted on a PCB substrate, showing a cut section corresponding to line IV-IV in FIG. **14** (an example where balls BMP (NC) are non-connected to a rewiring layer MRD).

FIG. **19** is a schematic sectional view of a semiconductor device in which a semiconductor package according to an embodiment is mounted on a PCB substrate, showing a cut section corresponding to line IV-IV in FIG. **14** (an example where BMPs are removed).

FIG. **20**A is a schematic view for explaining a pitch length of the balls corresponding to FIG. **18** or **19** and FIG. **20**B is a schematic view for explaining a pitch length of lands LND and wirings corresponding to FIG. **20**A.

FIG. **21** is a planar pattern configuration view of a semiconductor package according to an embodiment, showing BGA in which 10×8 solder bumps BMP each having the diameter D of 0.25L are arranged at a 2D (=0.5L) pitch on a surface of a side on which the solder bumps are formed.

FIG. **22** is a planar pattern configuration view showing a land LND forming surface of a PCB substrate on which the semiconductor package shown in FIG. **21** is mounted.

FIG. **23** is a planar pattern configuration view of a semiconductor package according to an embodiment, showing BGA in which 10×8 solder bumps BMP each having the diameter D of 0.2L are arranged at a 2D (=0.4L) pitch on a surface of a side on which solder bumps are formed.

FIG. **24** is a planar pattern configuration view showing a land LND forming surface of a PCB substrate **200** on which the semiconductor package shown in FIG. **23** is mounted.

FIG. **25** is a planar pattern configuration view of a semiconductor device according to an embodiment, showing BGA in which 10×8 solder bumps BMP each having the diameter D of 0.15L are arranged at a 2D (=0.3L) pitch on a surface of a side on which the solder bumps BMP are formed.

FIG. **26** is a planar pattern configuration view showing a land LND forming surface of a PCB substrate on which the semiconductor package shown in FIG. **25** according to an embodiment is mounted.

FIG. **27**A is a planar pattern configuration view of a semiconductor package according to a comparative example, showing BGA in which 5×5 solder bumps BMP each having the diameter D of 0.25L are arranged at a 2D (=0.5L) pitch.

FIG. **27**B is a planar pattern configuration view showing a land LND forming surface of a PCB substrate on which the semiconductor package shown in FIG. **27**A according to the comparative example is mounted.

FIG. **28** is a planar pattern configuration view showing a land LND forming surface of a PCB substrate on which a semiconductor package according to an embodiment is mounted, with lands LND arranged at a 0.4L pitch on the land LND forming surface.

FIG. **29** is a planar pattern configuration view showing a land LND forming surface of a PCB substrate on which a semiconductor package according to a comparative example is mounted, with lands LND arranged at a 0.4L pitch on the land LND forming surface.

FIG. **30** is a planar pattern configuration view showing a land LND forming surface of a PCB substrate on which a semiconductor package according to an embodiment is mounted, with lands LND arranged at a 0.3L pitch on the land LND forming surface.

DETAILED DESCRIPTION

Embodiments of the present disclosure will now be described in detail with reference to the drawings. Throughout the drawings, the same or similar elements are denoted by the same or similar reference numerals. It is, however, noted that the drawings are only schematic and the relationship between thickness and planar dimension, a layer thickness ratio and so on are unrealistic. Therefore, specific thicknesses and dimensions should be determined in consideration of the following description. In addition, it is to be understood that the drawings may include different portions of dimensional relations and ratios.

The following embodiments are illustrative of devices and methods for embodying the technical idea of the present disclosure and embodiments of the present disclosure are not intended to limit material, shapes, structures, arrangements and the like to those described below. The embodiments of the present disclosure may be modified in different ways without departing from the scope defined in the claims.

In addition, in the following embodiments, a semiconductor integrated circuit formed on a silicon wafer is also referred to as an LSI (Large Scale Integration), a package in which the LSI is accommodated is referred to as a semiconductor package, and the entire configuration where the semiconductor package is disposed on a PCB substrate is referred to as a semiconductor device. A semiconductor package with an LSI packaged therein may be a grid array package such as WL-CSP, BGA/LGA or the like.

[Basic Technique]

(Semiconductor Package)

FIG. **1** is a schematic bird's-eye view of a WL-CSP type semiconductor package **100**A according to the basic technique, which is seen from a front surface side facing a surface on which solder bumps BMP are formed. FIG. **2** is a schematic sectional view taken along line I-I in FIG. **1**, showing an example of solder bumps BMP formed of BGA. FIG. **3** is a schematic sectional view taken along line I-I in FIG. **1**, showing an example of solder bumps BMP formed of LGA.

The WL-CSP type semiconductor package **100**A will be described with reference to FIGS. **1** to **3**.

The WL-CSP type semiconductor package **100**A is a semiconductor package **100**A in which terminals and wirings (distinguished from LSI wirings and hereinafter, referred to as a "rewiring layer MRD") are formed before individual LSIs **10** are cut out from a silicon wafer with the LSIs **10** mounted thereon and, thereafter, on which the LSIs **10** cut out from the wafer are mounted.

The main reason for using the WL-CSP type semiconductor package is the minimization of the external size of the LSIs **10** (including thinness, lightness, a degree of freedom of terminal arrangement of the LSIs **10**, and so on) and particularly is the point that the external size of the LSIs **10** becomes the external size of the semiconductor package **100**A.

As shown in FIGS. **1** to **3**, the semiconductor package **100**A is substantially rectangular when viewed from top and has a plurality of solder bumps BMP provided as external terminals at predetermined intervals.

The semiconductor package **100**A includes a semiconductor integrated circuit (LSI) **10**, an interlayer film **12** formed on the front surface of the LSI **10**, a rewiring layer MRD formed on the interlayer film **12**, a protective layer (interposer) **14** covering the rewiring layer MRD, post electrodes MP formed respectively in openings looking into the rewiring layer MRD of the protective layer **14**, and solder bumps (balls) BMP disposed respectively on the post electrodes MP.

Here, the protective layer **14** is provided to cover the rewiring layer MRD and the post electrodes MP.

In addition, a mold resin layer **16** may be disposed, for example, via an LSI protective layer **27**, on the rear surface facing the front surface of the LSI **10** on which the protective layer **14** is formed.

The protective layer **14** may be made of, for example, epoxy resin. In addition, the rewiring layer MRD and the post electrodes MP are both formed of a metal layer.

(Semiconductor Device)

FIG. **4** is a schematic sectional view showing a state of disposing the semiconductor package **100**A on a PCB substrate **200**A according to the basic technique.

Here, the PCB substrate **200**A includes an insulating substrate **32** and lands LND arranged on the insulating substrate **32**. The PCB substrate **200**A may further include a wiring layer (not shown in FIG. **4**) disposed on the insulating substrate **32**. The insulating substrate **32** may be made of, for example, epoxy resin. The lands LND are formed of a metal layer.

The semiconductor package **100**A is disposed on the PCB substrate **200**A in such a manner that the solder bumps (balls) BMP disposed on the post electrodes MP face the lands LND disposed on the PCB substrate **200**A.

FIG. **5** is a schematic sectional view of a semiconductor device **300**A in which the semiconductor package **100**A is disposed on the PCB substrate **200**A. FIG. **6** is a schematic sectional view of another example of the semiconductor device **300**A in which the semiconductor package **100**A is disposed on the PCB substrate **200**A. FIG. **5** corresponds to a structure example of disposing BGA and FIG. **6** corresponds to a structure example of disposing LGA.

As shown in FIGS. **5** and **6**, the solder bumps (balls) BMP and the lands LND are fused together after being subjected to heat treatment and a resin layer **30** for protecting connection portions between the solder bumps (balls) BMP and the lands LND is formed between the semiconductor package **100**A and the PCB substrate **200**A.

FIG. **7** is a schematic plan view of the semiconductor package **100**A according to the basic technique, showing a surface of a side on which the solder bumps BMP are formed. FIG. **8** is a schematic plan view showing a surface of a side in which the lands LND of the PCB substrate **200**A mounting the semiconductor package **100**A are formed according to the basic technique introduced in FIG. **7**. Specifically, an insulating film is formed on the lands LND disposed on the insulating substrate **32** and openings of the insulating substrate **32** are connected to the solder bumps BMP. In FIG. **8**, peripheral portions EXT of the lands LND correspond to the insulating film.

FIG. **9** is a schematic enlarged view for explaining arrangements of the lands LND on the PCB substrate **200**. The lands LND (L_{11}, L_{12}, . . . , L_{21}, L_{22}, . . .) are arranged in the form of a square lattice on the insulating substrate **32** of the PCB substrate **200**. Assuming that the diameter of each land LND is D, a distance between adjacent lands LND is D and a pitch between the lands LND arranged in the form of a square lattice is represented by 2D.

FIG. **10** is a planar pattern configuration view of the semiconductor package **100**A according to the basic technique, showing BGA with balls arranged at a 0.5L pitch on a surface of a side on which the solder bumps BMP are formed.

Balls (solder bumps) B_{11}, B_{12}, . . . , B_{54} and B_{55} are arranged in the form of a square lattice on a solder bump BMP forming surface in the semiconductor package **100**A according to the basic technique. In the example shown in FIG. **10**, the diameter of each ball is 0.25L, a distance between adjacent balls is 0.25L, and an arrangement pitch between the balls is 0.5L. Where, L may be set to, for example, 1 mm.

FIG. **11** is a planar pattern configuration view of lands L_{11}, L_{12}, . . . , L_{54} and L_{55} arranged at a 0.5L pitch on a land LND forming surface of the PCB substrate **200**A on which the semiconductor package **100**A shown in FIG. **10** is mounted, and wirings W_{11}, W_{12}, . . . , W_{54} and W_{55} connected respectively to the lands L_{11}, L_{12}, . . . , L_{54} and L_{55}.

FIG. **12** is a schematic sectional view of the semiconductor device **300**A in which the semiconductor package **100**A according to the basic technique is disposed on the PCB substrate **200**A, showing a cut section corresponding to line III-III in FIG. **11**. In the semiconductor device **300**A in which the semiconductor package **100**A is disposed on the PCB substrate **200**A, since the semiconductor package **100**A is reversely disposed on the PCB substrate **200**A, the balls (solder bumps) B_{11}, B_{12}, . . . , B_{54} and B_{55} are arranged to face the lands L_{11}, L_{12}, . . . , L_{54} and L_{55} and are respectively connected to the lands L_{11}, L_{12}, . . . , L_{54} and L_{55}.

As shown in FIG. **12**, the balls (solder bumps) B_{11}, B_{12}, . . . , B_{54} and B_{55} are arranged to face the lands L_{11}, L_{12}, . . . , L_{54} and L_{55} and are respectively connected to the lands L_{11}, L_{12}, . . . , L_{54} and L_{55}.

As shown in FIG. **12**, the solder bumps (balls) B_{15}, B_{25}, . . . , B_{45} and B_{55} and the lands L_{11}, L_{12}, . . . , L_{54} and L_{55} are respectively fused together by heat treatment. In addition, a resin layer **30** for protecting connection portions between the solder bumps (balls) B_{15}, B_{25}, . . . , B_{45} and B_{55} and the lands L_{11}, L_{12}, . . . , L_{54} and L_{55} is formed between the semiconductor package **100**A and the PCB substrate **200**A.

EMBODIMENT

FIG. **13** is a planar pattern configuration view of the semiconductor package **100** according to an embodiment, showing BGA with balls arranged at a 0.4L pitch on a surface of a side on which solder bumps are formed.

Balls (solder bumps) B_{11}, B_{12}, . . . , B_{55} and B_{56} are arranged in the form of a lattice on a solder bump BMP forming surface when the protective layer **14** is viewed from top. The lattice may be one of a square lattice, a rectangular lattice, a triangular lattice and a hexagonal lattice. In addition, the arrangement example of FIG. **13** corresponds to an example of a square lattice.

In FIG. **13**, of the balls arranged in the periphery, the balls B_{13}, B_{14}, B_{31}, B_{36}, B_{53} and B_{54} are removed.

In the example shown in FIG. **13**, the diameter of each ball is 0.2L, a distance between adjacent balls is 0.2L, and an arrangement pitch between the balls is 0.4L. Where, L may be set to, for example, 1 mm.

FIG. **14** is a planar pattern configuration view of lands L_{11}, L_{12}, . . . , L_{55} and L_{56} arranged at a 0.4L pitch on a land LND forming surface of the PCB substrate **200** on which the semiconductor package **100** according to an embodiment is mounted, and wirings W_{11}, W_{12}, . . . , W_{55} and W_{56} connected respectively to the lands L_{11}, L_{12}, . . . , L_{55} and L_{56}.

Here, of the balls arranged in the periphery, the balls B_{13}, B_{14}, B_{31}, B_{36}, B_{53} and B_{54} are removed. That is, lands L_{13}, L_{14}, L_{31}, L_{36}, L_{53} and L_{54} corresponding to the removed balls B_{13}, B_{14}, B_{31}, B_{36}, B_{53} and B_{54} are removed.

As shown in FIG. **14**, a space of the removed lands L_{13} and L_{14} is used as a space for arrangement of the wiring W_{25}, W_{24} and W_{23}, a space of the removed land L_{36} is used as a space for arrangement of the wiring W_{35} and W_{45}, and a space of the removed lands L_{54} and L_{53} is used as a space for arrangement of the wiring W_{44}, W_{43} and W_{42}.

In some embodiments, balls arranged in corners and in the central portion of the solder bump BMP forming surface of the semiconductor package **100** and lands facing the balls may not be removed in order to secure connectivity between the semiconductor package **100** and the PCB substrate **200**.

That is, as shown in FIGS. **13** and **14**, in some embodiments, lands L_{11}, L_{16}, L_{51} and L_{56} arranged in the corners of the semiconductor device **300**, their corresponding balls B_{11}, B_{16}, B_{51} and B_{56}, lands L_{33} and L_{34} arranged in the central portion, and their corresponding balls B_{33} and B_{34} may be left in order to secure connectivity between the semiconductor package **100** and the PCB substrate **200**.

In addition, for the purpose of passing wirings of balls arranged in the inside and their corresponding lands, the lands L_{13}, L_{14}, L_{31}, L_{36}, L_{53} and L_{54} arranged in the periphery of the chip are removed. In addition, their corresponding balls B_{13}, B_{14}, B_{31}, B_{36}, B_{53} and B_{54} are also removed. In addition, the balls B_{13}, B_{14}, B_{31}, B_{36}, B_{53} and B_{54} corresponding to the removed lands L_{13}, L_{14}, L_{31}, L_{36}, L_{53} and L_{54} may have a non-contact (NC) configuration.

FIG. **16** is a schematic sectional view of the semiconductor device **300** in which the semiconductor package **100** according to an embodiment is disposed on the PCB substrate **200**, showing a cut section corresponding to line II-II in FIG. **14**. As shown in FIG. **16**, balls B_{53} and B_{54} are removed. In the example shown in FIG. **16**, lands L_{53} and L_{54} corresponding to the balls B_{53} and B_{54} are also removed.

As a modification, FIG. **15** is a schematic sectional view of a cut section corresponding to line II-II in FIG. **14**. In the example shown in FIG. **15**, the balls B_{53} and B_{54} are shown as BMP (NC) non-connected to the rewiring layer MRD. In the example shown in FIG. **15**, the lands L_{53} and L_{54} corresponding to the balls B_{53} and B_{54} are also removed. On the other hand, the lands L_{53} and L_{54} corresponding to the balls B_{53} and B_{54} may be left on the insulating substrate **32** and may be used as a part of the wirings.

As shown in FIGS. **13** to **16**, the semiconductor package **100** according to the embodiment includes a semiconductor integrated circuit **10**, an interlayer film **12** formed on the semiconductor integrated circuit **10**, a rewiring layer MRD formed on the interlayer film **12**, post electrodes MP formed on the rewiring layer MRD, a protective layer **14** which is formed on the interlayer film **12** and covers the rewiring layer MRD and the post electrodes MP, and balls BMP which are disposed respectively on the post electrodes MP and are connected to the rewiring layer MRD.

In addition, balls BMP (B_{13}, B_{14}, B_{31}, B_{36}, B_{53} and B_{54}) existing on a wiring path of internal wirings W_{22}, W_{23}, W_{24}, W_{25}, W_{32}, W_{35}, W_{42}, W_{43}, W_{44} and W_{45} that are connected to the inner lands LND (L_{22}, L_{23}, L_{24}, L_{25}, L_{32}, L_{35}, L_{42}, L_{43}, L_{44} and L_{45}) of a plurality of lands LND is arranged on the PCB substrate **200** to face a plurality of balls BMP, and the plurality of balls BMP may also be non-connected to the rewiring layer MRD.

Here, as shown in FIG. **15**, the protective layer **14** is interposed between the rewiring layer MRD and the balls BMP (B_{13}, B_{14}, B_{31}, B_{36}, B_{53} and B_{54}) non-connected to the rewiring layer MRD, so as to make a non-connection therebetween.

In addition, as shown in FIG. **16**, the balls BMP (B_{13}, B_{14}, B_{31}, B_{36}, B_{53} and B_{54}) existing on the wiring path of the internal wirings W_{22}, W_{23}, W_{24}, W_{25}, W_{32}, W_{35}, W_{42}, W_{43}, W_{44} and W_{45} connected to the inner lands LND (L_{22}, L_{23}, L_{24}, L_{25}, L_{32}, L_{35}, L_{42}, L_{43}, L_{44} and L_{45}) of the plurality of lands

LND which is arranged on the PCB substrate **200** to face the plurality of balls BMP and can be connected to the plurality of balls BMP may be removed.

As shown in FIGS. **13** to **16**, the PCB substrate **200** according to the embodiment includes an insulating substrate **32**, a plurality of lands L_{11}, L_{12}, . . . , L_{55} and L_{56} which are arranged on the insulating substrate **32** to face a plurality of balls B_{11}, B_{12}, . . . , B_{55} and B_{56} of the semiconductor package **100** and can be respectively connected to the plurality of balls B_{11}, B_{12}, . . . , B_{55} and B_{56}, and wirings W_{11}, W_{12}, . . . , W_{55} and W_{56} which are arranged on the insulating substrate **32** and are respectively connected to the plurality of lands L_{11}, L_{12}, . . . , L_{55} and L_{56}.

In addition, as shown in FIGS. **13** to **16**, the lands LND (L_{13}, L_{14}, L_{31}, L_{36}, L_{53} and L_{54}) existing on a wiring path of internal wirings W_{22}, W_{23}, W_{24}, W_{25}, W_{32}, W_{35}, W_{42}, W_{43}, W_{44} and W_{45} connected to lands LND (L_{22}, L_{23}, L_{24}, L_{25}, L_{32}, L_{35}, L_{42}, L_{43}, L_{44} and L_{45}) which are arranged in the inside on the insulating substrate **32** are removed.

In addition, the lands LND (L_{13}, L_{14}, L_{31}, L_{36}, L_{53} and L_{54}) may be used as non-contact lands LND (NC) by being non-connected to the rewiring layer MRD of the semiconductor package **100**. In this case, the lands LND (NC) (L_{13}, L_{14}, L_{31}, L_{36}, L_{53} and L_{54}) may be left on the insulating substrate **32** and may be used as a part of wirings.

The lands L_{11}, L_{12}, . . . , L_{55} and L_{56} are arranged in the form of a lattice when the insulating substrate **32** is viewed from top. The lattice may be one of a square lattice, a rectangular lattice, a triangular lattice and a hexagonal lattice.

In some embodiments, lands L_{11}, L_{16}, L_{51} and L_{56} arranged in corners of the insulating substrate **32** and lands L_{33} and L_{34} arranged in the central portion may be left in order to secure connectivity with the semiconductor package **100**.

As shown in FIGS. **13** to **16**, the semiconductor device **300** according to the embodiment includes a semiconductor package **100** including a semiconductor integrated circuit **10**, an interlayer film **12** formed on the semiconductor integrated circuit **10**, a rewiring layer MRD formed on the interlayer film **12**, post electrodes MP formed on the rewiring layer MRD, a protective layer **14** which is formed on the interlayer film **12** and covers the rewiring layer MRD and the post electrodes MP, and balls BMP which are disposed respectively on the post electrodes MP and are connected to the rewiring layer MRD; and a PCB substrate **200** including an insulating substrate **32**, lands LND which are arranged on the insulating substrate **32** to face balls BMP and can be connected to the balls BMP, and wirings W which are arranged on the insulating substrate **32** and are connected to the lands LND.

Here, the balls BMP (B_{13}, B_{14}, B_{31}, B_{36}, B_{53} and B_{54}) existing on a wiring path of internal wirings W_{22}, W_{23}, W_{24}, W_{25}, W_{32}, W_{35}, W_{42}, W_{43}, W_{44} and W_{45} that are connected to lands LND (L_{22}, L_{23}, L_{24}, L_{25}, L_{32}, L_{35}, L_{42}, L_{43}, L_{44} and L_{45}) are arranged in the inside of the insulating substrate **32** may be removed or be non-connected to the rewiring layer MRD.

Here, as shown in FIG. **15**, the protective layer **14** is interposed between the rewiring layer MRD and the balls BMP (B_{13}, B_{14}, B_{31}, B_{36}, B_{53} and B_{54}) non-connected to the rewiring layer MRD, making non-connection therebetween.

In addition, in some embodiments, balls arranged in the corners and the central portion of the semiconductor package **100** may be left in order to secure connectivity with the PCB substrate.

The semiconductor package **100** may be a wafer level chip size package.

FIG. **17**A is a schematic view for explaining a pitch length of the balls corresponding to FIG. **15** or **16** and FIG. **17**B is a

schematic view for explaining a pitch length of the lands LND and the wirings W and WS corresponding to FIG. **17**A.

Two BMP portions indicated by a broken line in FIG. **17**A indicates that they are BMP(NC) in non-contact with the rewiring layer MRD or are removed. For example, the two BMP portions indicated by the broken line correspond to the removed balls B_{13} and B_{14} or the removed balls B_{53} and B_{54} in FIG. **13**.

In this manner, when the two BMP portions indicated by the broken line have a space of 1.0L between BMPs in both sides and three wirings W pass therebetween, line-and-spaces of L/7 are obtained as shown in FIG. **17**B. On the other hand, as shown as a comparative example in the left side of FIG. **17**B, when one thin wiring WS passes in a space of 0.2L between lands LND, a line-and-space of 0.2L/3 is obtained. That is, the wiring width is about 2.1 times and there is no need to miniaturize the wiring width on the PCB substrate.

FIG. **18** is a schematic sectional view of the semiconductor device **300** in which the semiconductor package according to an embodiment is disposed on the PCB substrate, showing a cut section corresponding to line IV-IV in FIG. **14**. An example where a ball corresponding to the ball B_{36} has BMP (NC) in non-contact with the rewiring layer MRD is shown in FIG. **18**. The land L_{36} corresponding to the ball B_{36} is removed.

FIG. **19** is a schematic sectional view of the semiconductor device **300** in which the semiconductor package according to an embodiment is disposed on the PCB substrate, showing a cut section corresponding to line IV-IV in FIG. **14**. As shown in FIG. **19**, a ball corresponding to the ball B_{36} is removed. The land L_{36} corresponding to the ball B_{36} is also removed.

FIG. **19** is a schematic sectional view of the semiconductor device **300** in which the semiconductor package **100** according to an embodiment is disposed on the PCB substrate **200**, showing a cut section corresponding to line IV-IV in FIG. **14**. As shown in FIG. **19**, the ball B_{36} is removed. The land L_{36} corresponding to the ball B_{36} is also removed in the example shown in FIG. **19**.

As a modification, FIG. **18** is a schematic sectional view of a cut section corresponding to line II-II in FIG. **14**. In the example shown in FIG. **18**, the ball B_{36} is shown as BMP(NC) non-connected to the rewiring layer MRD. In the example shown in FIG. **18**, the land L_{36} corresponding to the ball B_{36} is also removed. On the other hand, the land L_{36} corresponding to the ball B_{36} may be left on the insulating substrate **32** and may be used as a part of the wirings.

FIG. **20**A is a schematic view for explaining a pitch length of the balls corresponding to FIG. **18** or FIG. **19** and FIG. **20**B is a schematic view for explaining a pitch length of the lands LND and the wirings W corresponding to FIG. **20**A.

One BMP portion indicated by a broken line in FIG. **20**A indicates that it is BMP(NC) in non-contact with the rewiring layer MRD or is removed. For example, the one BMP portion indicated by the broken line corresponds to the removed ball B_{31} or B_{36} in FIG. **13**.

In this manner, when one BMP portion indicated by the broken line has a space of 0.6L between BMPs in both sides and two wirings W pass therebetween, line-and-spaces of 0.12L are obtained as shown in FIG. **20**B. On the other hand, as shown as a comparative example in the left side of FIG. **20**B, when one thin wiring WS passes in a space of 0.2L between lands LND, a line-and-space of 0.2L/3 is obtained. That is, the wiring width is about 1.8 times and there is no need to miniaturize the wiring width on the PCB substrate.

FIG. **21** is a planar pattern configuration view of the semiconductor package **100** according to an embodiment, showing BGA in which 10×8 solder bumps BMP each having the diameter D of 0.25L are arranged at a 2D (=0.5L) pitch on a surface of a side on which the solder bumps BMP are formed. FIG. **22** is a planar pattern configuration view showing a land LND forming surface of the PCB substrate **200** on which the semiconductor package **100** shown in FIG. **21** is mounted.

As shown in FIG. **21**, since the plurality of bumps BMP is arranged on a trajectory consisting of four hierarchies, i.e., rounds R**1**, R**2**, R**3** and R**4**, balls BMP existing on a wiring path of an internal wiring connected to a land disposed in the inner side need be removed or be non-connected.

As one example, the balls BMP (B_{51}, B_{52} and B_{53}) existing on a wiring path of the internal wiring W_{44} connected to the land L_{44} disposed in the inner side on the insulating substrate **32** are removed or non-connected to the rewiring layer MRD. In addition, the lands LND (L_{51}, L_{52} and L_{53}) facing the balls BMP (B_{51}, B_{52} and B_{53}) are removed or are non-connected.

Similarly, FIG. **23** is a planar pattern configuration view of the semiconductor package **100** according to an embodiment, showing BGA in which 10×8 solder bumps BMP each having the diameter D of 0.2L are arranged at a 2D (=0.4L) pitch on a surface of a side on which the solder bumps BMP are formed. FIG. **24** is a planar pattern configuration view showing a land LND forming surface of the PCB substrate **200** on which the semiconductor package **100** shown in FIG. **23** is mounted.

As one example, the balls BMP (B_{83}, B_{93} and B_{103}) existing on a wiring path of the internal wiring W_{74} connected to the land L_{74} disposed in the inner side on the insulating substrate **32** are removed or non-connected to the rewiring layer MRD. In addition, the lands LND (L_{83}, L_{93} and L_{103}) facing the balls BMP (B_{83}, B_{93} and B_{103}) are removed or are non-connected.

Similarly, FIG. **25** is a planar pattern configuration view of the semiconductor package **100** according to an embodiment, showing BGA in which 10×8 solder bumps BMP each having the diameter D of 0.15L are arranged at a 2D (=0.3L) pitch on a surface of a side on which the solder bumps BMP are formed. FIG. **26** is a planar pattern configuration view showing a land LND forming surface of the PCB substrate **200** on which the semiconductor package **100** shown in FIG. **25** is mounted.

As one example, the balls BMP (B_{66}, B_{67} and B_{68}) existing on a wiring path of the internal wiring W_{75} connected to the land L_{75} disposed in the inner side on the insulating substrate **32** are removed or non-connected to the rewiring layer MRD. In addition, the lands LND (L_{66}, L_{67} and L_{68}) facing the balls BMP (B_{66}, B_{67} and B_{68}) are removed or are non-connected.

In any arrangements, the balls BMP (B_{11}, B_{18}, B_{101}, B_{108}, B_{54}, B_{55}, B_{64} and B_{65}) arranged in the corners and central portion of the semiconductor package **100** are preferably left in order to secure connectivity with the PCB substrate **200**. The semiconductor package **100** may be a wafer level chip size package.

(Reduction of Chip Size)

FIG. **27**A is a planar pattern configuration view of the semiconductor package **100**A according to a comparative example, showing BGA in which 5×5 solder bumps BMP each having the diameter D of 0.25L are arranged at a 2D (=0.5L) pitch. FIG. **27**B is a planar pattern configuration view showing a land LND forming surface of the PCB substrate **200**A on which the semiconductor package **100**A shown in FIG. **27**A is mounted. When the semiconductor package **100**A is a wafer level chip size package, the chip size of the semiconductor integrated circuit **10** is substantially the same as the size of the semiconductor package **100**A. Therefore, the chip size of the semiconductor integrated circuit **10** accommodated in the semiconductor package **100**A according to the comparative example is equal to 2.5L×2.5L.

FIG. **28** is a planar pattern configuration view showing a land LND forming surface of the PCB substrate **200** on which the semiconductor package **100** according to an embodiment is mounted, with lands LND each having the diameter D of 0.2L arranged at a 2D (=0.4 L) pitch on the land LND forming surface. The chip size of the semiconductor integrated circuit **10** accommodated in the semiconductor package **100** disposed on the PCB substrate **200** shown in FIG. **28** is equal to 2.0L×2.4L.

When the pitch of the solder bumps BMP each having a diameter D of 0.25L, is 0.5L, since 22 pins are required, the chip size becomes at least 2.5L×2.5L and the wiring pitch may be 0.25L singly. On the other hand, when the pitch of solder bumps BMP each having the diameter D of 0.2L, is 0.4L, the chip size can be reduced and the wiring pitch can meet the conditions of 0.25L per pitch, as shown in FIG. **28**. Therefore, the chip area can be reduced without having an effect on the PCB substrate cost. The minimum chip size at this time is 2.0L×2.4L which is reduced to about 23%.

FIG. **29** is a planar pattern configuration view showing a land LND forming surface of the PCB substrate **200**A on which the semiconductor package **100**A according to a comparative example is mounted, with lands LND each having the diameter D of 0.2L arranged at a 2D (=0.4L) pitch on the land LND forming surface. The chip size of the semiconductor integrated circuit **10** accommodated in the semiconductor package **100**A disposed on the PCB substrate **200**A shown in FIG. **29** is equal to 2.0L×2.0L.

FIG. **30** is a planar pattern configuration view showing a land LND forming surface of the PCB substrate **200** on which the semiconductor package **100** according to an embodiment is mounted, with lands LND each having the diameter D of 0.15L arranged at a 0.3L pitch on the land LND forming surface. The chip size of the semiconductor integrated circuit **10** accommodated in the semiconductor package **100** disposed on the PCB substrate **200** shown in FIG. **30** is equal to 1.5L×1.8L.

When the pitch of the solder bumps BMP each having a diameter D of 0.2L, is 0.4L, since 22 pins are required, the chip size becomes at least 2.0L×2.0L and the wiring pitch may be 0.2L per pitch. On the other hand, when the pitch of the solder bumps BMP each having the diameter D of 0.15L, is 0.3L, the chip size can be reduced and the wiring pitch can meet the conditions of a 0.2L per pitch, as shown in FIG. **30**. Therefore, the chip area can be reduced without having an effect on PCB substrate cost. The minimum chip size at this time is 1.5L×1.8L and this reduces the size to about 32%.

In the semiconductor package **100** according to the embodiment, it is possible to alleviate the ball arrangement pitch rule and reduce the chip size of the semiconductor integrated circuit **10**. That is, the ball arrangement pitch rule may be alleviated from 0.5L to 0.4L (L is an arbitrary constant). Alternatively, the ball arrangement pitch rule may be alleviated from 0.4L to 0.3L (L is an arbitrary constant).

On the other hand, the PCB substrate **200** on which the semiconductor package according to the embodiment can be easily mounted without requiring miniaturization of wiring width on the PCB substrate.

In addition, since the chip size of the semiconductor integrated circuit can be reduced, the semiconductor package can be downsized.

In the semiconductor package according to the embodiment, the PCB substrate on which the semiconductor package is mounted, and the semiconductor device including the PCB substrate and the semiconductor package mounted on the

PCB substrate, when WL-CSP/BGA/LGA is mounted on the PCB substrate, balls corresponding to lands acting as necks to pass wirings on the PCB substrate are removed or made in non-contact (NC).

With the semiconductor package according to the embodiment, the land portion corresponding to the removed balls can be used as wirings on the PCB substrate, thereby narrowing a ball pitch and a land pitch corresponding to the balls. As a result, the chip size can be reduced. In addition, the land portion corresponding to the removed balls can also be removed, in which case the removed corresponding portion can be used as a space for wirings on the PCB substrate.

With the semiconductor package according to the embodiment, the land portion corresponding to the non-contacted balls can be used as wirings on the PCB substrate, thereby narrowing a ball pitch and a land pitch corresponding to the balls. As a result, the chip size can be reduced.

In addition, as for the wiring pitch, it is possible to secure a space of the same level as conventional, thereby preventing increase in PCB substrate cost, which can result in reduction in the entire system cost.

As described above, according to this embodiment, it is possible to provide a semiconductor package which is capable of reducing the chip size and eliminating a need to miniaturize the wiring width on a PCB substrate and can be easily mounted, a PCB substrate on which the semiconductor package is mounted, and a semiconductor device including the PCB substrate and the semiconductor package mounted on the PCB substrate.

The semiconductor package and semiconductor device of the present disclosure may be applied to WL-CSP type semiconductor devices, QNF package type semiconductor devices, and so on.

According to the present disclosure in some embodiments, it is possible to provide a semiconductor package which is capable of reducing the chip size and eliminating a need to miniaturize the wiring width on a PCB substrate and can be easily mounted, a PCB substrate on which the semiconductor package is mounted, and a semiconductor device including the PCB substrate and the semiconductor package mounted on the PCB substrate.

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosures. Indeed, the novel methods and apparatuses described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the disclosures. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosures.

What is claimed is:

1. A semiconductor device comprising:

a semiconductor package including a semiconductor integrated circuit, an interlayer film disposed on the semiconductor integrated circuit, a rewiring layer disposed on the interlayer film, post electrodes disposed on the rewiring layer, a protective layer which is disposed on the interlayer film and covers the rewiring layer and the post electrodes, and a plurality of balls which is respectively disposed on the post electrodes and is connected to the rewiring layer; and

a printed circuit board substrate including an insulating substrate, a plurality of lands which is arranged on the insulating substrate to face the plurality of balls and is respectively connectable to the plurality of balls, and wirings which are arranged on the insulating substrate and are respectively connected to the plurality of lands,

wherein balls existing on a wiring path of internal wirings, which are connected to lands arranged in the inside on the insulating substrate, are removed,

wherein the internal wirings are formed between balls adjacent to each other when viewed from top, and

wherein between the adjacent balls, a center of the rewiring layer and centers of the internal wirings deviate from each other when viewed from top.

2. The semiconductor device of claim **1**, wherein the plurality of balls are arranged in a form of a lattice when the protective layer is viewed from top.

3. The semiconductor device of claim **2**, wherein the lattice is one of a square lattice, a rectangular lattice, a triangular lattice and a hexagonal lattice.

4. The semiconductor device of claim **1**, wherein an arrangement pitch rule of the plurality of balls is allowed to be alleviated to reduce a chip size of the semiconductor integrated circuit.

5. The semiconductor device of claim **4**, wherein the arrangement pitch rule of the plurality of balls is alleviated from 0.5L to 0.4L (L is an arbitrary constant).

6. The semiconductor device of claim **4**, wherein the arrangement pitch rule of the plurality of balls is alleviated from 0.4L to 0.3L (L is an arbitrary constant).

7. The semiconductor device of claim **1**, wherein balls arranged in corners and a central portion of the semiconductor package are not removed so that connectivity with the printed circuit board substrate is secured.

8. The semiconductor device of claim **1**, wherein the semiconductor package is a wafer level chip size package.

9. A semiconductor device, comprising:

a semiconductor package including a semiconductor chip having a first front surface and a first rear surface, a rewiring layer formed on the first front surface of the semiconductor chip and electrically connected with the semiconductor chip, and a plurality of electrodes formed on the rewiring layer and electrically connected with the rewiring layer; and

a substrate having a second front surface, which faces the first front surface, and a second rear surface, the substrate including wirings respectively connected to the plurality of electrodes, the wirings being formed on the second front surface from an inside of a portion facing the semiconductor package to an outside of a periphery of the portion facing the semiconductor package,

wherein the rewiring layer and the wirings are formed between electrodes adjacent to each other when viewed from top such that a center of the rewiring layer and centers of the wirings deviate from each other.

10. The semiconductor device of claim **9**, wherein between the adjacent electrodes when viewed from top, the wiring layer and the wirings partially overlap.

11. The semiconductor device of claim **10**, wherein between the adjacent electrodes when viewed from top, an area of the rewiring layer not overlapping with the wirings is larger than an area of the rewiring layer overlapping with the wirings.

12. The semiconductor device of claim **9**, wherein between the adjacent electrodes when viewed from top, the rewiring layer is interposed between two or more wirings.

13. The semiconductor device of claim **9**, wherein the rewiring layer and the wirings are spaced apart from each other when viewed from top.

14. The semiconductor device of claim 13, wherein between the adjacent electrodes when viewed from top, the rewiring layer is interposed between two or more wirings.

15. The semiconductor device of claim 9, wherein between the adjacent electrodes when viewed from top, a plurality of dummy electrodes, which is physically spaced apart from the rewiring layer, is formed to overlap with the rewiring layer.

16. The semiconductor device of claim 15, wherein an insulating layer is formed between the rewiring layer and the plurality of dummy electrodes.

17. The semiconductor device of claim 9, wherein the plurality of electrodes is arranged in a form of a lattice when viewed from top.

18. The semiconductor device of claim 17, wherein the lattice is one of a square lattice, a rectangular lattice, a triangular lattice and a hexagonal lattice.

19. The semiconductor device of claim 9, wherein an arrangement pitch rule of the plurality of electrodes is allowed to be alleviated to reduce a chip size of the semiconductor integrated circuit.

20. The semiconductor device of claim 19, wherein the arrangement pitch rule of the plurality of electrodes is alleviated from 0.5L to 0.4L (L is an arbitrary constant).

21. The semiconductor device of claim 19, wherein the arrangement pitch rule of the plurality of electrodes is alleviated from 0.4L to 0.3L (L is an arbitrary constant).

22. The semiconductor device of claim 9, wherein electrodes arranged in corners and a central portion of the semiconductor package are not removed so that connectivity with the printed circuit board substrate is secured.

23. The semiconductor device of claim 9, wherein a part of distances between adjacent wirings is same.

24. The semiconductor device of claim 9, wherein the semiconductor package has a pair of first sides facing each other when viewed from top and a pair of second sides facing each other when viewed from top, the second sides being shorter than the first sides, and

wherein the plurality of electrodes is arranged in a plurality of electrode rows along an elongate direction of the first sides, and in at least two electrode rows, a region where the center of the rewiring layer and the centers of the wirings deviate from each other when viewed from top is interposed between adjacent electrodes.

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